Current Mode Wave Active Filters. A topology for integrated high frequency filters

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Contents

Principal mathematical symbols

A	Incident wave
B	Reflected wave
V	Voltage
I	Current
R	Resistance value
C	Capacitance value
L	Inductance value
$\mathbf{S}$	Scattering parameter matrix
$\mathbf{Y}$	Admittance matrix
s	The complex frequency
Q	Quality factor for second order biquad transfer function
ω	Resonance frequency of second order biquad transfer function. Also, imaginary part of complex frequency (corresponds to physical signals)
σ	Real part of complex frequency
Z', Z''	Impedances in Lattice prototype section
S', S''	Transfer functions in Lattice simulation two–pair
N	Turns ratio in ideal transformer
$h(s)$	Transfer function
τ	Time constant in first–order integrator
α, β	Contributions to first order two–pair transfer function
K_1, K_2	Gain constants in first order two–pair transfer function

$\tau\prime$	Effective time constant in first order two–pair
τ_d	Time constant for HF rolloff for current duplicator
G_{di}, G_{do}	Input and output admittances of current duplicator
G_{go}	Output conductance of OTA
τ_L, τ_C	Actual time constant values for inductance and capacitance simulating two–pairs
O(x^n)	Remainder in Taylor expansion, goes to zero for $x \to 0$ proportionally to x^n
Q_0, ω_0	Ideal values of biquad characteristics
$\hat{Q}$	Inverse of relative bandwidth in lowpass – bandpass frequency transform
$\tilde{s}$	Bandpass frequency point
$\tilde{\omega}_+$	Larger bandpass frequency defined by lowpass frequency ω and frequency transform
$\tilde{\omega}_-$	Smaller bandpass frequency defined by lowpass frequency ω and frequency transform
T_i	Transistor number i
V_{dd}	Positive supply voltage
V_{ss}	Negative supply voltage
V_T	Threshold voltage for FET transistor
V_D	Maximum gate–source voltage for GaAs transistor
V_{GS}	Gate–source voltage for FET transistor
V_{DS}	Drain–source voltage for FET transistor
C_{GS}	Gate–source parasitic capacitance for FET transistor
L	Gate length for FET transistor
I_D	Drain current in FET transistor
f_T	Unity gain frequency for an individual transistor in current amplifier configuration
V_{bi}	Bias voltage index i

V_{in}	Input voltage
I_{in}	Input current
I_o	Output current
K	Constant in FET square law $I_D(V_{GS})$ characteristic (and all–purpose constant...)
F_0	Denormalisation frequency for filter
P	Power consumption of filter
D	Dynamic range for filter
l', l'', m	Inductances in Lattice equivalent
c_a, c_b	Capacitances in ditto
R_s, R_l	Source and load resistances
Q^H	Quality factor for transfer function pole–pair
Q^B	Quality factor for biquad transfer function
$\mathbf{P}$	Left transformation matrix in Linear Transformation analysis
$\mathbf{Q}$	Right transformation matrix ditto
$\mathbf{T}$	Modified Chain matrix for prototype in Linear Transformation analysis
$\mathbf{C}$	Modified Chain matrix for building block in Linear Transformation analysis

Chapter 1

Introduction

This thesis describes the novel filter topology *Current Mode Wave Active* (CMWA). This topology is offered as an alternative to traditional impedance simulation topologies for integrated Continuous–Time filters operating at high frequencies.

1.1 Original contribution

Since the CMWA filter topology was introduced by myself, most of the material in this thesis is original. This means that, apart from the material described in the review chapter and the wave filter analysis material, the filter synthesis material is original. The circuit techniques used to implement the CMWA filters are not original, but picked out of the literature at random. To wit, the main points of the CMWA topology are

- In contrast to traditional OTA–C filters, two types of active devices are used. Also, for each elementary block in the prototype filter, there are two sets of in/out connections which are not tied to any impedance level (in traditional OTA–C filters there is only one set of in/out connections, but they are tied to the filter impedance level).

- The simulation of the reactive branches of doubly terminated LC filters is performed from a description talking into account the resistive loss in the termination, i.e. with either lossy first order integrators of low–Q biquads as the frequency dependent processing elements.

- The simulation of some four terminal circuits, such as the balanced Lattice section, is possible. In the Lattice section simulation, allpass filters are used; these may be realised with the same building blocks as used for the simulation of traditional elements (e.g. it is possible to simulate high order allpass functions using interconnected first order lossy integrators).

- For filters based on first order integrators, the DC gain of the amplifiers does not have to be very large (since it is possible to compensate for the effects of the loss by tuning amplifier gain). Likewise, it is possible to compensate for the effects of high frequency rolloff by tuning amplifier gain.

- For the one complete CMWA chip I have made so far, measurements confirm the theoretical points.

1.2 Description of the study

Since the final product of any PhD work is determined in no small part by the practical aspects of the work, a few discussions of the work follows. The project started in the fall of -90 and ended in the first months of -94 (including the time taken to write the thesis).

1.2.1 Discussion of original project description

The original project sprang from the continuing work of my supervisor in the field of linear lumped Gallium Arsenide Giga–Hertz circuits. The idea was that my knowledge of filters should combine with his knowledge of the low–level issues involved in GaAs circuits to produce integrated tunable high–performance filters for microwave frequencies. While the motivation for such a project was sound enough, the actual project turned out to be unrewarding. As the theoretical work progressed, it turned out that the practical work were going to be fraught with difficulty — because of the features of the available process and because of facilities. Because the practical goals would be difficult to reach, and because of the more wide reaching theoretical implications of the new CMWA filter topology, the GaAs project was quietly laid to rest.

1.2.2 Brief chronological overview of study

The project started off with a false start, in that some months were spent on a filter analysis/synthesis computer program. The practical software engineering aspects absorbed a lot of time, and in the end the program was not very useful for the filter work, since most of the problems would be solved by a symbolic math program (as outlined in appendix B). After this period the literature study of existing work on integrated filters — mainly in CMOS technology — and GaAs circuits went smoothly. On the more practical front, some design workshops/courses with the Eurochip GaAs group at the Rutherford Appleton Lab introduced me to the particular problems of GaAs chip design. While some theoretical work on lumped integrated GaAs filtering was progressing at various universities around the world, very little practical work was being discussed in the literature. Ref. [1.2] is typical of the papers being published in the field. The paper [1.1] was the only paper published through this period, and was not very relevant to the main strand of my work.

After about a year, I decided to read fully, and understand, the first reference I had found on Wave Active filters, ref. [1.4]. The synthesis method held some fascination for me, so I tracked down some of the referenced papers, notably [1.10], where a simpler approach was taken. After some time, the CMWA basic block, the two–pair (a two–input two–output first order lossy integrator), was found. With the realisation that I had found a new filter topology which differed markedly from those in use in integrated filters, I started to work exclusively in this area. The first CMWA paper [1.7] was written in a hurry, and as a consequence contained an unfortunate assumption which makes the "practical" example of little interest.

The next half year was spent doing several transistor level designs of CMOS CMWA filters. Two complete chips were laid out, but only the last (the design described in detail in [1.6]) was actually fabricated. A transistor level design of the basic building blocks in GaAs technology was carried out, but proved to be quite unsatisfactory. After the CMOS chip was finally sent off, I discovered the Lattice simulation blocks and produced a paper [1.9] on the subject. Further work lead to the next paper [1.8] and to the summer of -93. A paper submitted to IEEE Transactions CAS took up the rest of the time spent before the thesis was started.

1.3 Typography notes

This thesis was typeset with the program LaTeX. The various typefaces, and their meaning in this thesis, are

Name	Purpose	Sample
Plain	Used for normal text	
Mathematical	Mathematical elements:	
	scalars	V_1, S_{ij}, ε
	vectors, matrices	$\mathbf{S}$, $\mathbf{V^n}$
	Captions in figures	T_1, V_{DD}
Emphasised	Definitions of terms	*Wave*
Typewriter	Computer program names, input, etc	`HSPICE`, `Solve[]`

For a vector $\mathbf{V}$ the notation $\mathbf{V^n}$ signifies the vector with index n, whereas V_n signifies the nth element in the vector $\mathbf{V}$. For a matrix, any index for the entire matrix is positioned as superscript, allowing for both indexing of matrices *and* identification of specific columns in a matrix, i.e. $\mathbf{S^i}$ is $\mathbf{S}$ matrix with index i and $\mathbf{S^i_2}$ is the second column of that matrix and S_{ij} is the element in row i column j of matrix $\mathbf{S}$. Apart from an inverse matrix — which is still signified by $\mathbf{M^{-1}}$ for matrix $\mathbf{M}$ — no use of matrices raised to a power is made in this thesis; it is understood that no index -1 is used (i.e. $\mathbf{M^{-1}}$ always signifies inversion of $\mathbf{M}$) and that the inverse of matrix $\mathbf{M^i}$ is denoted $(\mathbf{M^i})^{-1}$.

1.4 Contents of this thesis

Since conventional OTA–C filters are just that, there are many good studies (although mainly in PhD theses, e.g. [1.5, 1.3]) of the area as such. Nonetheless, chapter 2 gives a brief review of the literature about integrated continuous–time filters for the applications for which I feel that CMWA filters would be applicable, followed by a brief description of previous Continuous–Time Wave Active filters. Chapter 3 gives the basic (known) analysis/synthesis theory behind Wave Active filters. Chapter 4 describes the new Current Mode Wave Active filter topology; giving first a simple description of the building blocks and then going into the theory of practical use in some detail. To strengthen the argument in favour of CMWA filters, practical results are needed; chapter 5 gives descriptions of the performance of a fabricated CMOS filter and of various simulated circuits. Chapter 6 wraps up the thesis.

A few words about what this thesis does *not* contain. Since the CMWA filter topology was discovered in the course of this study, a lot of time was spent in understanding the fundamentals. Consequently, some of the really involved analysis has not been done because of time constraints. Although the title of this thesis mentions "high frequency" there is actually no measured results for filters running at extremely high frequencies. The aspects of operating at high frequencies are discussed in some depth, and the measured results bear out the main conclusions about problems with high frequency operation. The main emphasis in the work behind the thesis was to discover as many new and exiting aspects of the topology as such. Hence the modest effort in the experimental part, where only one filter was completed.

1.5 Acknowledgements

I would like to extend my warm thanks to my supervisor *Dr Chris Toumazou* for his contribution. He provided me with the right amount of freedom to do my own thing (which led me to find a new topology) while at the same time providing a focusing influence to keep the work more or less on the right track (for instance, he goaded me into doing the work that led to the discovery that amplifier gain tuning alters the Q of the complete filters). My funding agency, the Danish Technical Research Council (*Statens Teknisk–Videnskabelige Forskningsråd*), was most helpful in making sure that I did my best, and in making certain that I had the funding to perform the practical activities so important for the work (fabricating chips, attending conferences). In particular, my "daily" contacts, Ole Schwarz and Peter Grønborg, were very encouraging. As indicated in section 6.2, a monograph by Dr Wupper, reference [1.11], came into my possesion at the last minute; I would like to thank Dr Wupper for letting me have a copy of this important source.

For the experimental work, I am grateful to the many poeople who helped me with various practical issues connected to analogue VLSI. My fellow students N Battersby and M Cheng, M Brent of the University of London VLSI Consortium and D Wadsworth, G Swanson, P Mole and P Mannas of BNR/nt provided assistance with the actual design/fabrication issues.

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Chapter 2

Review of OTA–C and Wave Active–RC filters

This chapter gives a brief overview with literature references of the state of the art in in the field of integrated Continuous–Time filters simulating LC prototypes. For historical completeness, a description of the original work in discrete Wave Active–RC filters is also given together with a description of the only other integrated Wave Active filter.

LC ladder filters are chosen as prototypes because of their low sensitivity to changes in reactive component values[1]. In general, only unbalanced LC ladders are used as prototypes but we give a few examples of prototype structures which are not simple LC ladders. Continuous–Time integrated filters have two main areas of application: before/after Discrete–Time signal processing elments at any frequency and in high frequency applications where Discrete–Time implementations are not possible [2.47]. The first application is perhaps the one liable to be most relevant in the long run, as the limit for operational speed of Discrete–Time signal processing keeps increasing [2.25, 2.24].

[1]While cascades of low order elements are also commonly used, the sensitivity properties are not as good as those of LC ladder simulations (with a factor 1000 in sensitivity cited [2.34] for one example)

The original Active–RC Wave filters operate with resistors, capacitors, voltage buffers and operational amplifiers. While such implementations work well for low frequency applications, they do not represent a clear advantage over other Active–RC structures. Because of the nature of these implementations, they are not well suited for integrated implementations.

2.1 Integrated OTA–C filters

The purpose of LC filter simulations is to avoid the use of inductors in the final filter, often because the final filter is to be built as an integrated circuit. The basis of the filter simulations is the approach taken in describing the prototype filter. While the operation of the complete LC filter can be described by two variables (the input and the output) and the transfer function, we wish to simulate the method by which the transfer function is defined, i.e. the operation of the individual LC elements in the prototype. The various LC filter simulations chose different sets of state variables to describe the prototype, and therefore arrive at different (or not so different) results.

The most popular class of LC simulations are impedance simulations, in which only one electrical variable is chosen for each prototype element (the branch current or voltage drop) as a state variable. By a sensible choice of variables, a set of equations using only integration as the frequency dependent operation can be found. From such a set of equations, a circuit consisting of interconnected integrators may be built. While the various synthesis methods are firmly rooted in the relevant analysis method, the results are often equivalent. The methods of embedding (the gyrator–C method) [2.14] and leapfrog (SFG) synthesis [2.16] can lead to identical circuits via radically different analysis/synthesis routes (this equivalence is noted in [2.8]). Most often, the prototype filter is an unbalanced ladder structure taken from a reference book like [2.40] where standard solutions are listed. From reference works, it is possible to find the smallest (most economical) solution given a set of performance specifications. Traditionally, the performance of the prototype is maximally flat approximation (Butterworth functions for amplitude, Bessel functions for group delay) or equi–ripple approximation (elliptical functions for amplitude, no known solution for group delay). The tabulated solutions are all lowpass filters which are transformed to highpass or bandpass filters if necessary.

2.1.1 Implementation issues

Given an LC ladder prototype, the task of making an OTA–C simulation seems fairly simple. In reality, there are numerous problems, leading to the fact that OTA–C filtering has only recently become an established field with a certain industrial relevance [2.47]. Many problems are caused by the limitations of the actual implementation, e.g. a desire to have a filter on a digital chip where the noise in the supply lines (and in the substrate) makes a balanced design necessary. More general limits are defined by the fact that there is, *for linear filters*, a fundamental limit on the performance, given by the fact that the performance measures are connected; e.g. for a bandpass biquad the relation [2.47, section 6] $P = KQ\omega_0 D$ with P the power, K a design dependent constant, ω_0 and Q the usual and D the dynamic range[2].

Implementation problems divide into, among others: topology issues, linear performance of OTA, nonlinear performance of OTA and the tuning process. In the following paragraphs, we give a few conclusions from the current state of the art (*caveat emptor*, as the field is constantly evolving).

Topology issues are the problems in selection of detailed simulation subcircuits and nominal values for capacitance and transconductance. In an inte-

[2] An example is [2.30, section 6.3] where a television IF filter was designed. The transfer function specification was within reach, but the dynamic range specification would require an increase in power consumption by a factor 500

grated environment, all capacitors and amplifiers will have parasitic capacitors to the substrate. These capacitances are difficult to match and are not necessarily very linear and, first of all, may introduce capacitances where there is not supposed to be any [2.15]. For this reason, it is advantageous to have a topology with capacitors from all nodes to ground, and no floating capacitances. This is, unfortunately, only trivially the case for simulation of polynomial lowpass filters, all other filters having floating capacitors in the prototype. While topologies with minimum number of amplifiers need to implement floating capacitors explicitly (and may have nodes with no capacitances to ground), it is possible — by increasing the number of amplifiers — to simulate the floating capacitances using gyrator circuits (or different formulations of the SFG equations) [2.14, 2.44]. Having all OTAs identical — tuned to identical transconductance — leads to particularly simple design procedures; this is also advisable for a number of not so obvious reasons: the overlap capacitances have no effect and the sensitivity is minimal for passive gyrators (gyrators where the two OTAs are identical) [2.30, chapters 2,3]. Unfortunately, this will lead to unacceptably large capacitance value spreads in narrow band bandpass filters; in this case a narrow band approximation — implementable with coupled resonators — is the better solution [2.28] but does require OTAs with different values. Amplitude scaling concerns may also indicate that OTAs with different values are desirable [2.16].

The linear performance criteria for OTAs are the frequency limits and the parasitic output impedance (parasitic capacitances are assumed absorbed by the topology). For the integrators the integration has to be lossless, since the reactive prototype elements are lossless. Any deviation from lossless integration is equivalent to resistive loss in the prototype, an error to which LC ladders — and any simulations — are quite sensitive [2.37]. For filters operating over a wide frequency range (i.e. lowpass or highpass filters), the approximation to lossless integration is difficult to maintain. At low frequencies, the finite DC gain of the OTA caused by the finite output impedance will introduce phase lead errors and at high frequencies the finite bandwidth of the OTA will introduce phase lag errors. The effects of these errors are discussed in, among others, references [2.13, 2.32, 2.12, 2.2]. Only in bandpass filters is it practical to compensate for phase lag by using tunable phase lead (as suggested in [2.46, 2.26]); for wide band applications the effects must be compensated for by separate means. Often, the DC gain is increased by using output cascoding in the OTAs or by inserting small negative conductances in parallel with the output [2.31]. The effect of high frequency rolloff can be compensated for by inserting a tunable zero in the integrator transfer function; either a tunable RC combination in the input stage, acting as a variable degeneration resistor [2.49] or a resistor between ground and the integration capacitor [2.51, 2.21].

The nonlinear performance criteria for OTAs are the distortion, the rejection of supply noise and common mode signals and the generated noise. The commonly accepted way of reducing the distortion and increasing the rejection of unwanted signals is to use a balanced structure and symmetrical signals. The responses of the CMOS transistor enable very linear amplifiers to be built for symmetrical operation. Since frequency performance is always a major consideration, the simpler amplifier structures are almost always preferable, e.g. [2.43, 2.54, 2.31, 2.23]. Although some form of common mode feedback scheme has to be employed to control the DC operating point, balanced operation seems to be the necessary choice for high performance integrated filters. For balanced operation the filter topology is usually identical to that for unbalanced operation (apart from the trivial doubling of circuitry) apart from the fact that inversion is accomplished more simply (by switching signals over). Since the field of OTA design is so large with many diverse methods, the only conclusion made here is that balanced operation is best and that simpler circuits are better.

The necessary tuning process is one of the greater practical problems. Because of the physical fabrication process, there are large variations for some physical parameters, leading to large systematic variations for time constants of the form G_m/C. These variations are usually assumed to be identical for all parts of the chip and up to $\pm 15\%$. Thus, for all but the least demanding applications[3] some form of tuning is required to get the centre/cutoff frequency of the filter set to the specified value. By nature of their design, most integrated Continuous–Time filters are frequency tunable. The tuning range may, however, be only just large enough to enable the filter to operate correctly at one frequency; this is typically the case for CMOS technology filters where many critical performance measures vary with tuning, i.e. it is difficult to make a CMOS filter operate well over a large tuning range (say, larger than a factor two). Tuning circuits divide into two groups: master–slave and non master–slave. The master–slave (MS) scheme tunes one subcircuit (typically a bandpass biquad) to perform correctly and transmits the tuning quantities to the rest of the filter which is supposed to match "sufficiently well". A common implementation is to tune a bandpass biquad to be perfectly lossless using a phase detector and an amplitude detector separately with one frequency input. The phase detector detects exactly $90°$ phase shift (centre frequency) and the amplitude detector detects unity gain (losslessness). Referred to as a T_{12} tuning scheme in [2.48] this will tune biquads with very high Q factors; if lower Q factors are required — with precision — a more complex scheme has to be used. Early integrated filters would use either MS [2.26] or other schemes, e.g. the multi–frequency scheme reported in [2.35]. Later, most filters would use MS tuning; the present opinion [2.47] is that MS is fine for noncritical filters but that more complex schemes are necessary for high performance. A number of schemes using multiple tuning measurements (e.g. tuning individual biquads separately) have been reported [2.20, 2.5]. The disadvantage of this approach is that the filter is unusable while being tuned (since the signal path is broken); this might not be a great problem in some

[3]One example [2.39] uses a Continuous–Time filter for input antialiasing filter before a Discrete–Time highpass filter; only the lowerq cutoff frequency is critical and the upper cutoff frequency is insignificant — thus no tuning is necessary for the Continuous–Time filter

systems (e.g. for digital communication and storage systems) where there are well defined pauses between data and well defined procedures for retrying on failed operation. Other complicated methods analyse the relation between input and output for the complete filter, either computing the correlation functions for the two signals, as in [2.7], or sending a reference signal into the filter and comparing to a pre–computed expected output, as in [2.27]. While these methods require extensive computational effort for the tuning, they may represent the only option for designs where the highest quality is required. Generally speaking, MS is recommended for its simplicity of implementation, with various very complicated schemes necessary for demanding applications. (With extremely careful design, MS can be made to work very well indeed, as shown in reference [2.50].)

2.1.2 Non–traditional filters

While simulation of unbalanced LC ladders dominate the field of low sensitivity filter synthesis[4] (i.e. where cascades of biquads are impractical), there are several other methods. In order to achieve low sensitivity, topologies are "very interconnected" — i.e. all reactive components affect all transfer function pole values — and pseudo–passive — i.e. contain no sections with power gain. A trivial example is bandpass filters built from coupled resonators [2.26, 2.49]. More involved examples use regular structures such as "Follow–the–Leader" and "multiloop" feedback schemes, e.g. reference [2.28]. Using the LC ladder prototype to write up a set of equations which are then simulated with a large number of capacitors and a small number of amplifiers is described in [2.22]. Common to all these "different" methods is that the transfer functions are still of the type that can be implemented with unbalanced LC ladders (i.e. minimum phase transfer functions without multiple poles).

[4] A few specific examples where cascade realisations have lower sensitivity — often using transfer functions with multiple poles — have been put forward, e.g. [2.4]

The traditional way to build a linear phase filter is to design a filter to implement the required amplitude transfer function (using a standard solution) and cascade with a phase equaliser having allpass transfer function. The phase equalisers are either cascades of biquad sections or "ladder–type" allpass filters [2.9], compared in [2.38]. Since this method only extends the available transfer functions to include allpass factors, there is still a large number of transfer function families to explore. Some attempts have been made at designing transfer functions that are not minimum phase and which do not contain allpass factors, e.g. references [2.3, 2.42, 2.55]; and explorations of the relation between linear phase and amplitude selectivity for minimum phase filters have appeared, e.g. [2.10, 2.41]. Apart from a few papers on active–RC solutions, e.g. [2.36], interest in simulation of ladder–type circuits with non minimum phase transfer function without allpass factors seems to be non existent, apart from the present contribution — e.g. [2.45].

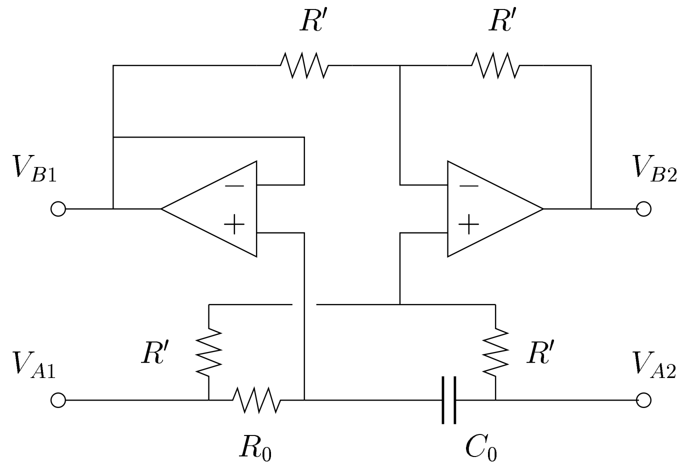

Figure 2.1: Active–RC two–pair simulating series capacitor

2.2 Previous work in Wave Active–RC filters

Continuous–Time structures based on Wave analysis of LC ladder filters followed soon after the initial digital structures [2.19]. Two distinct approaches are taken, filters based on direct implementation of the **S** matrices [2.52, 2.53] and filters based on Wave Adaptors [2.6, 2.1] (reference [2.11] proposes one circuit of each kind). A later paper [2.29] generalised the Wave Active design procedure by starting with the transfer function and using first and second order blocks as necessary, including the ability to simulate a wider range of transfer functions (i.e. transfer functions which may be non minimum phase). A more general analysis framework [2.17] leads to a synthesis procedure which has both leapfrog and Wave Active synthesis methods as special cases. From [2.11] we have appropriated the term *Wave Active* and from [2.29] the term *two–pair*.

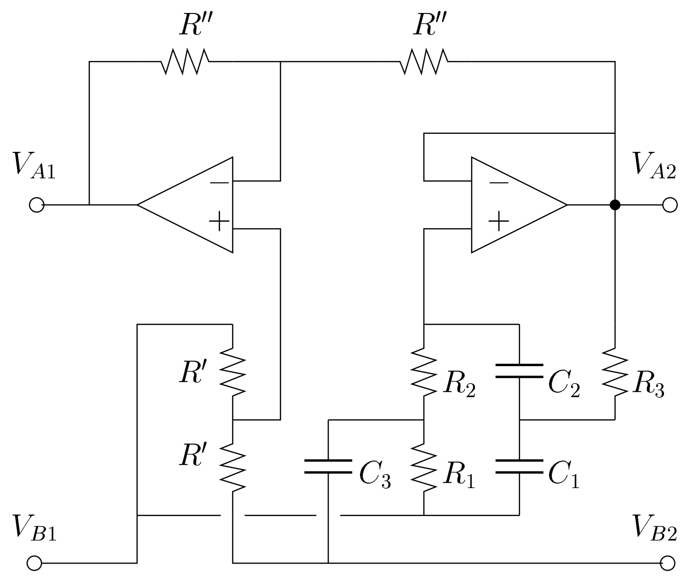

Figure 2.2: Active–RC two–pair simulating series resonance circuit

The direct simulation of **S** matrices, specifically the Wave Active simulation of a series capacitor, leads to an Active–RC circuit shown in figure 2.1. (Another circuit using only voltage buffers is proposed, but this circuit uses two identical capacitors to create the time constant.) The time constant is given by $\tau = R_0C_0$. In the same vein, an Active–RC two–pair simulating a series parallel resonator (the second entry in table 3.2) is shown in figure 2.2. The resistors marked R' and R'' simply provides feedback for the op–amps, so they may be set to any value.

The Wave Adaptor based synthesis uses Active–RC circuits to generate the wave signals from reactive subcircuits. It is possible to use either resistive adaptors or adaptors employing capacitors. Capacitive adaptors are used to achieve impedance transformation allowing the reactive subcircuits to be simulated with resistors. A resistive adaptor and a capacitive adaptor is shown in figure 2.3. Note that the downwards connectors are connected directly to the prototype elements (or the impedance transformed equivalent). Thus, it is possible to simulate inductors using adaptors and to use capacitors directly, thus mixing impedance simulation and Wave Active simulation. The resistor R in the resistive adaptor and the C capacitor in the capacitive adaptor have values which are used in forming the time constant; the R' resistor merely provide feedback for the op–amp. A section of a LC polynomial bandpass filter, and simulation in the styles of [2.6] (termed New Wave Active Adaptor) and [2.1] (termed Wave Active Adaptor), is shown in figure 2.4.

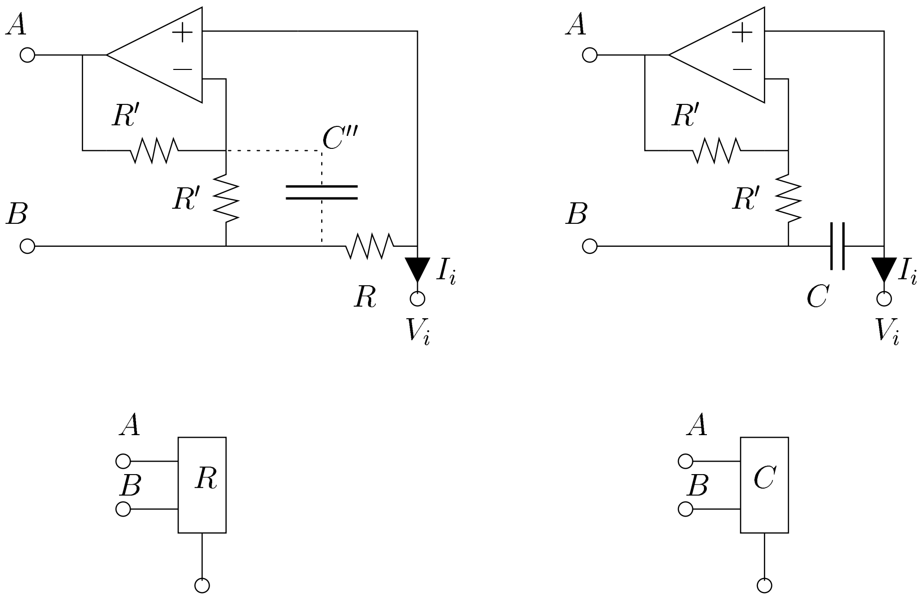

Figure 2.3: Wave adaptors (R and C types) and corresponding symbols. The R type is shown with compensation capacitor C''

The Wave Adaptor filters use reactive elements loaded by the system impedance and may employ floating capacitors. The V_i and I_i quantities in figure 2.3 are

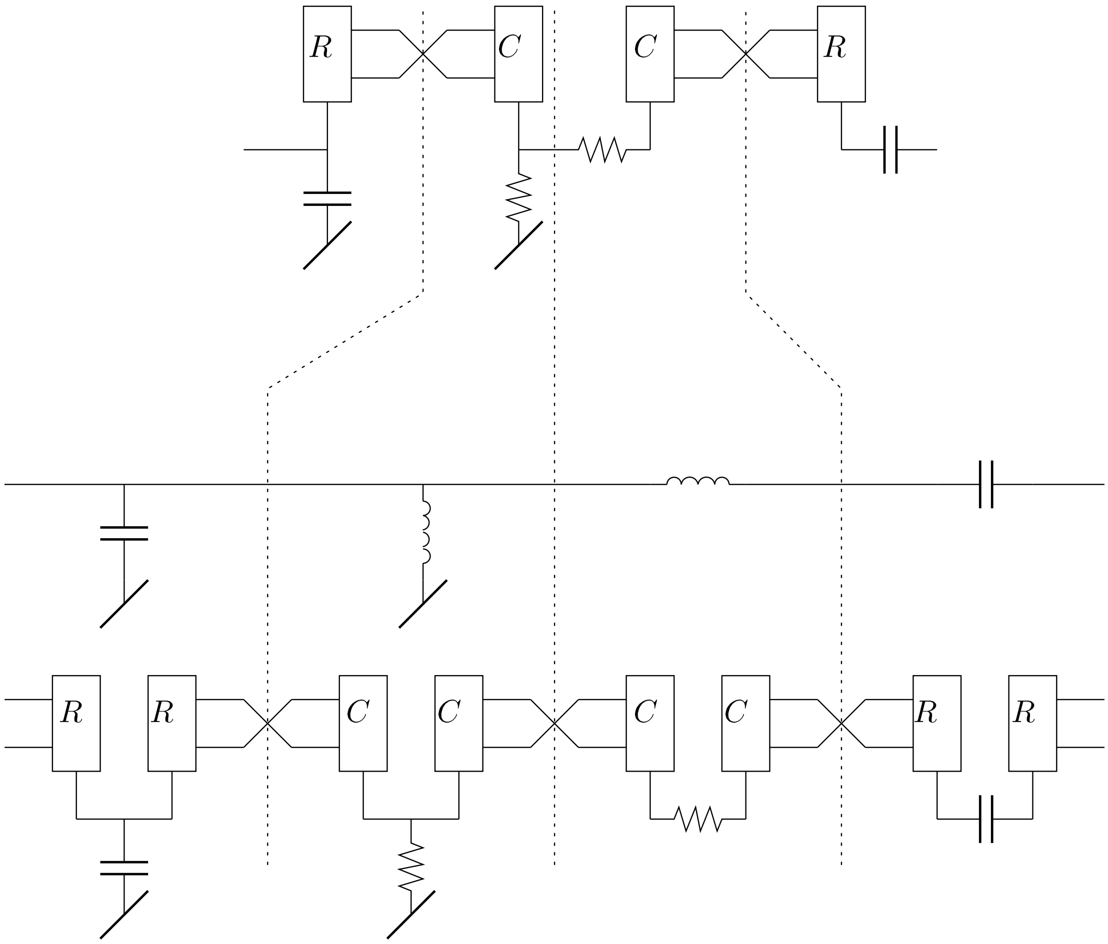

Figure 2.4: Polynomial bandpass prototype sections (middle), New Wave Active Adaptor simulation (top) and Wave Active Adaptor simulation (bottom)

the same as in the prototype (or impedance–scaled versions of the signals), therefore lossless operation is required. In [2.1] a derivation of the effect of finite op–amp gain–bandwidth (GB) product is performed, and it is demonstrated that a compensation is possible by inserting a capacitor (marked C'' in figure 2.3). This compensation allows operation at very high frequencies (the example in the paper is a lowpass filter with cutoff frequency of 1/10 of the opamp GB frequency).

2.2.1 Previous integrated Wave Active filters

Two integrated filters related to Wave Active filter synthesis have appeared. One, a silicon BJT filter, is a voltage mode Wave Active filter [2.33] and is described below. The other filter describes itself as implementing a new filter principle and illustrates this with a Signal Flow Graph (SFG) corresponding to a Wave Active filter; unfortunately, the shown implementation seems to deviate from the SFG. This filter is described in appendix D.

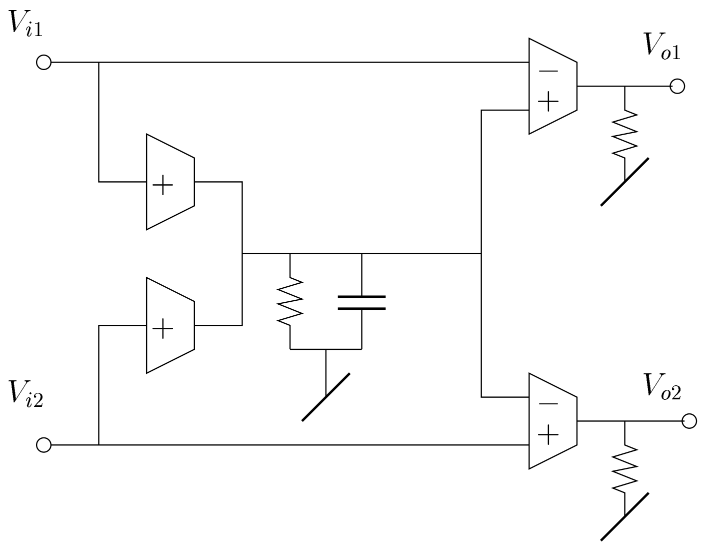

Figure 2.5: Voltage Mode Wave Active two–pair

The silicon filter in [2.33] uses roughly the same structure as CMWA filters, i.e. the filter consists of two–input two–output building blocks, each using a lossy integrator as the frequency dependent processing element. The Wave signals are voltage, with the topology of a two–pair shown in figure 2.5. The two–pair has the transfer functions (3.14) except that the input terminals are switched around and there is an inverter at the reflection input. The time constant is determined by a resistor–capacitor parallel combination, with the resistor realised on–chip and the capacitor an off–chip device (in the prototype); for a future fully integrated version, tunable capacitors are proposed. For an elliptical lowpass filter there are problems with the response in the stopband, but a novel prototype removing the infinite–frequency pole (by using several transformers) leads to a realisation without high frequency problems. The attractive simplicity of this circuit is due to the fact that tunable capacitors are proposed[5].

2.3 Discussion and Conclusion

Integrated Continuous–Time filters have achieved status as viable solutions to a range of real–world problems. Several filters with very high operating frequencies have been reported, e.g. a 98 MHz cutoff frequency 3rd order elliptical lowpass filter [2.31] and a biquad tunable to up to 450 MHz centre frequency [2.43]. Other performance measures, such as dynamic range and power consumption[6] may never be able to compare favourably with passive solutions; a complete system redesign would be needed before integrated filters could replace passive filters in many cases. The greatest difficulty in designing integrated Continuous–Time filters appears to be the tuning circuits in the case of high precision filters and the amplifier design in the case of high dynamic range filters.

The original work on Wave Active–RC filters spawned work in essentially two directions: direct implementation of S matrices with lossy integration as the elementary operation and the use of Wave Adaptors which generate wave signals from lossless reactive elements (or, equivalently, purely resistive elements). Common to both approaches is the reliance on floating resistors; for an integrated implementation active simulations would have to be used which would increase the complexity dramatically. It should also be noted

[5]The literature does not mention tunable capacitors for integrated filters very often, with one exception being [2.18], which is a filter operating at quite low frequencies (less than 100 KHz)

[6]for a system using passive filters: the power necessary to drive the in/out buffers operating at low impedances (e.g. 50 Ω) and the amplifiers to increase the signal level to compensate for insertion loss

that the excellent sensivitiy characteristics of the passive prototypes are only retained in the sensitivity to changes in the time constans, the resistors R' and R'' provide gain and any difference in values is equivalent to resistive loss in the prototype (as noted in [2.37]).

The existing integrated Wave Active filter exhibits some of the characteristics of the CMWA filters. High quality factor from amplifiers with low DC gain is the concrete result of using Wave Active synthesis. A drawback of this filter is that the varactor diodes used for frequency tuning are not usually considered sufficiently linear for normal quality criteria.

In this chapter we have given a brief summary of the state of the art in integrated Continuous–Time filters design and described previous work in Wave Active–RC filters. Integrated Continuous–Time filters appear to be a quite mature area, even if there are still many practical problems. Classical Wave Active–RC filters were not obviously better than the many different discrete impedance simulation strategies, while having the handicap of needing a design procedure which is "unusual".

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Chapter 3

Wave Active analysis/synthesis

Wave Active (WA) filters are a subclass of the general RLC filter[1] simulations. Where the basic state variables chosen in the prototype filters are traditionally combinations of node voltages and branch currents, WA filters use a linear combination of port voltages and port currents. The matrices defining the modification of these state variables are scaled versions of the conventional power scattering matrices. Hence, the state variables are called *waves*, although there is no connection to the physical waves appearing in various other prototype designs, e.g. surface waves or waves in distributed circuits.

This chapter describes briefly the known theory of WA synthesis (by way of analysis). It is shown how a conventional filter may be analysed as a series of building blocks and how each building block may be replaced by a WA filter element. This chapter serves as the basis for the CMWA synthesis described in the rest of thesis (and also as an introduction to a subject which is rarely touched upon in the literature).

[1] I am concerned solely with those linear lumped RLC filters which can be described as a cascade of reactive sections terminated by resistors. The simulations are all integrated linear continuous–time circuits

3.1 Wave description of LC filters

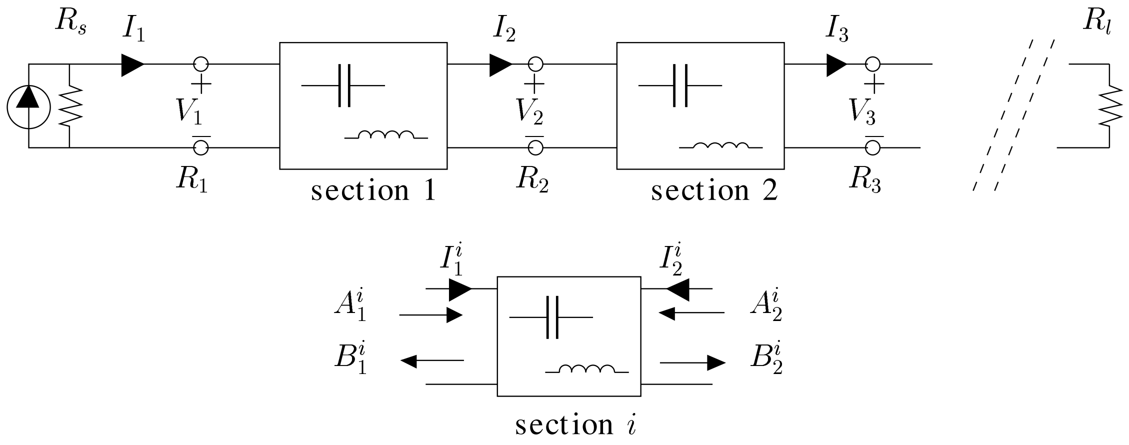


Figure 3.1: General RLC filter prototype with voltages V_i, currents I_i and impedance levels R_i for the port terminals. General section with waves

LC filters are chosen as prototypes because of the low sensitivity to changes in component values. The most common type of prototype is the unbalanced ladder structure, but we allow more general structures, such as those containing balanced Lattice structures. The prototypes are analysed as a cascade of reactive sections connected in series between a source terminal and a load terminal; two resistors loading the structure are connected at the terminals. The interconnections of the reactive sections define the *ports* where the quantities used to define the waves are calculated. Figure 3.1 shows a general prototype with definitions of port quantities: voltages, currents and impedance levels (the impedance levels are set arbitrarily, conventionally they are set to the source resistance value). Each block is a *two–port* which does not have to be a three–terminal but is a restricted class of four–terminal circuits[2]. For a general section we define the *incident* waves $A^i_{1/2}$ and the *reflected* waves $B^i_{1/2}$ from the port quantities.

Because the analysis for each isolated block sets the current into the section

[2]The restriction, as discussed in [3.2, chapter 17], is that the currents in the two terminals defining a port sum to zero

positive in both ends, the currents used in the definitions of the waves have the opposite sign every second time they appear in an equation. The waves for the first section of the filter are

$$\begin{bmatrix} A_1^1 \\ B_1^1 \end{bmatrix} = \begin{bmatrix} V_1 + R_1 I_1 \\ V_1 - R_1 I_1 \end{bmatrix}, \quad \begin{bmatrix} A_2^1 \\ B_2^1 \end{bmatrix} = \begin{bmatrix} V_2 - R_2 I_2 \\ V_2 + R_2 I_2 \end{bmatrix} \tag{3.1}$$

When analysing block i isolated, we introduce the currents I_1^i and I_2^i both positive into the block; thus we arrive at the chosen representation, the voltage waves $\mathbf{A}$ and $\mathbf{B}$ related by the voltage scattering matrix $\mathbf{S}$

$$\mathbf{V^i} = \begin{bmatrix} V_i \\ V_{i+1} \end{bmatrix} \quad \mathbf{I^i} = \begin{bmatrix} I_i \\ -I_{i+1} \end{bmatrix} \quad \mathbf{R^i} = \begin{bmatrix} R_i & 0 \\ 0 & R_{i+1} \end{bmatrix} \tag{3.2}$$

$$\mathbf{A^i} = \mathbf{V^i} + \mathbf{R^i I^i}, \quad \mathbf{B^i} = \mathbf{V^i} - \mathbf{R^i I^i} \tag{3.3}$$

$$\mathbf{B^i} = \mathbf{S^i A^i} \tag{3.4}$$

The equations (3.3) define the wave quantities as linear combinations of port voltages and currents. A generalised approach, Linear Transformation filter analysis/synthesis [3.3], is described in appendix C where a few variations on the equations above are also shown. The waves used here are voltage waves (since the dimension is voltage); using current waves would result in identical $\mathbf{S}$ matrices. In the rest of this thesis, the block index will usually be omitted from the equations as it is not significant when treating each block in isolation.

When computing the actual transfer function of a wave active filter, it is necessary to use a different matrix to indicate the operation of the sections, the *chain*[3] matrix Π, which is defined by

$$\begin{bmatrix} A_1 \\ B_1 \end{bmatrix} = \Pi \begin{bmatrix} B_2 \\ A_2 \end{bmatrix} \tag{3.5}$$

[3]As is the case for the $\mathbf{S}$ matrix, the chain matrix is defined differently in conventional usage

$$\Pi \;=\; \frac{1}{S_{21}}\begin{bmatrix} 1 & -S_{22} \\ S_{11} & S_{12}S_{21} - S_{11}S_{22} \end{bmatrix} \tag{3.6}$$

The transfer function for a given wave active filter is computed by taking the product of all chain matrices from right to left (reordering the result rows as necessary). The Π matrix for the complete filter defines the first input as function of the last output the inverse of this transfer function is the total transfer function. The **S** matrix is found from the Π matrix as follows

$$\mathbf{S} \;=\; \frac{1}{\Pi_{11}}\begin{bmatrix} \Pi_{21} & \Pi_{11}\Pi_{22} - \Pi_{12}\Pi_{21} \\ 1 & -\Pi_{12} \end{bmatrix} \tag{3.7}$$

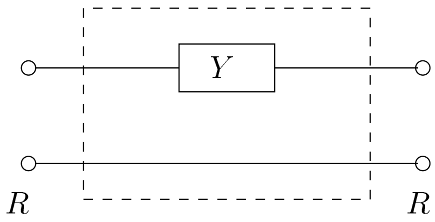


Figure 3.2: Series element with admittance Y

The **S** matrix is defined from the admittance matrix for a given subblock as follows

$$\mathbf{S} \;=\; 2(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \mathbf{RY})^{-\mathbf{1}} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.8}$$

For three–trerminal sections, the $\mathbf{Y}$ matrix above is the traditional definite admittance matrix. For two–ports which are not three–terminals, the $\mathbf{Y}$ matrix is defined using port voltages and currents (rather than terminal voltages/currents).

For a simple series admittance, as shown in figure 3.2, we get the following

$$\mathbf{S} \;=\; \frac{1}{1\,+\,2RY}\begin{bmatrix} 1 & 2RY \\ 2RY & 1 \end{bmatrix} \tag{3.9}$$

If the series element with the admittance Y is replaced by a series element with the admittance $Y' = 1/(4R^2Y)$, equation (3.9) changes to

$$\mathbf{S} \;=\; \frac{1}{1\,+\,2RY}\begin{bmatrix} 2RY & 1 \\ 1 & 2RY \end{bmatrix} \tag{3.10}$$

in other words, by interchanging the output terminals of a wave active subblock simulating the series admittance Y we get a wave active subblock simulating the series admittance $1/(4R^2Y)$. This technique will give us simulations of series capacitor elements from a simulation of a series inductor element. Another useful transformation is the insertion of a pair of gyrators around a given series admittance element. This is equivalent to having an element of the inverse admittance in shunt, as shown in figure 3.3. The $\mathbf{S}$ matrix for the gyrator with gyration resistance R is simply

$$\mathbf{S} \;=\; \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{3.11}$$

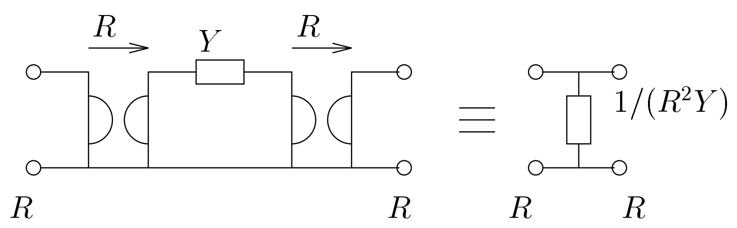


Figure 3.3: A series admittance between two gyrators and the equivalent shunt admittance

The final parts of the analysis needed before synthesis can be performed is the handling of interconnections and impedance levels. The $\mathbf{S}$ matrices shown so far have been computed under the assumption that the impedance level is identical in both ends of the reactive section; in this case interconnection is simply a matter of joining the terminals together. Input A_2^i is joined directly to output B_1^{i+1} and output B_2^i is joined to input A_1^{i+1}. If the impedance level changes at a port, a network must be inserted; either an ideal transformer or a matching network.

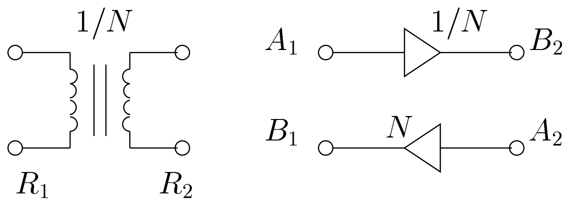


Figure 3.4: Ideal transformer ($R_2 = N^2 R_1$) and Wave equivalent

An ideal transformer is simulated as shown in figure 3.4. The **S** matrix of the ideal transformer with turns ratio N — connected between sections with impedance levels R and N^2R — is simply

$$\mathbf{S} = \begin{bmatrix} 0 & N \\ 1/N & 0 \end{bmatrix} \tag{3.12}$$

This use of the ideal transformer makes a lossless connection between sections of different impedance levels; it is typically used when it is desired to change component values, e.g. to reduce component value spread. A lossy connection must be simulated with a different network, the *matching* network. This is typically needed for lowpass filters of even order with Chebyshev passband characteristic where the level of gain at DC is different from 0.5, i.e. the load resistor is different from the source resistor and the resulting loss is part of the design. The **S** matrix of the matching network is

$$\mathbf{S} = \frac{1}{R_1 + R_2} \begin{bmatrix} R_2 - R_1 & 2R_1 \\ 2R_2 & R_1 - R_2 \end{bmatrix} \tag{3.13}$$

3.2 Simulation of LC filters

The CMWA filter synthesis process simply consists of writing up the S matrices for the reactive section and implementing those two–input two–output transfer functions as electronic circuits. Each block simulating an S matrix is called a *two–pair*. The structure of the two–pair depends on the structure of the prototype element(s) simulated; the obvious procedure is to use two–pairs with a first order integrator for first order sections, two–pairs with a bandpass biquad for second order sections and two–pairs with two second order circuits to simulate a balanced Lattice section containing second order impedances. If the impedance level is set to the source impedance, the only impedance related operation is the possible addition of a matching network at the output of the filter — in case the load impedance is different from the source impedance; all other interconnections between two–pairs are direct.

3.2.1 Simulation of plain ladder sections

The basic block chosen to be the elementary block for the first order integrator based implementations is the two–pair which simulates a series inductor L. The circuit is defined by the S matrix derived using (3.9):

$$\mathbf{S} = \frac{1}{1 + s\tau}\begin{bmatrix} s\tau & 1 \\ 1 & s\tau \end{bmatrix} \tag{3.14}$$

$$\tau = \frac{L}{2R} \tag{3.15}$$

The reason that the circuit defined by this prototype can be the elementary building block is that the other first order prototype elements can be simulated from this by either changing the outputs around (as ilustrated by equation (3.10)) to simulate the inverse admittance or by inserting inverters (simulating the insertion of a pair of gyrators) to simulate a shunt element. Table 3.1 shows the simulation of the first order building blocks from the two–pair with the $\mathbf{S}$ matrix (3.14).

Continuing the simulation of conventional LC elements, the use of a second order bandpass transfer function as the frequency dependent operation is described. Applying the conversion between $\mathbf{Y}$ matrix and $\mathbf{S}$ matrix, we arrive at the transfer function matrix for the two–pair simulating a parallel resonance circuit in a series branch

$$\mathbf{S} = \frac{1}{s^2 + s\,\omega/Q + \omega^2} \begin{bmatrix} s^2 + \omega^2 & s\,\omega/Q \\ s\,\omega/Q & s^2 + \omega^2 \end{bmatrix} \tag{3.16}$$

$$\omega = \sqrt{\frac{1}{LC}} \tag{3.17}$$

$$Q = \frac{1}{2R}\sqrt{\frac{L}{C}} \tag{3.18}$$

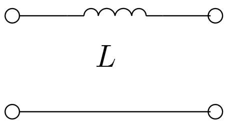
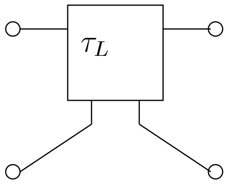
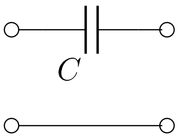
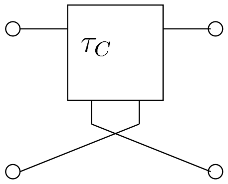
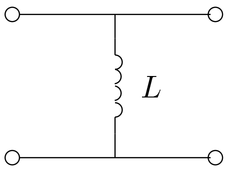
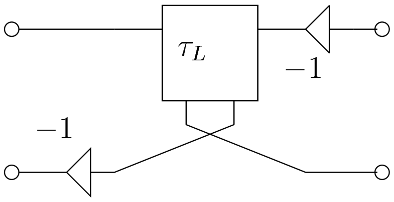
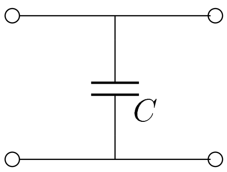
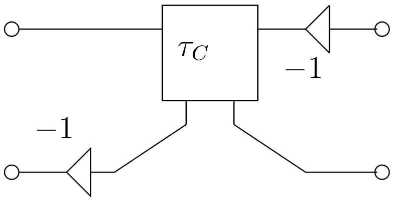
Prototype element	complete Two–pair	Time constant
		$\tau_L = L/(2R)$
		$\tau_C = 2RC$
		$\tau_L = 2L/R$
		$\tau_C = RC/2$

Table 3.1: First order prototype branches and corresponding two–pairs built from the first order elementary two–pair

The symbol for the second order two–pair and the corresponding prototype are given in the first row of table 3.2. While it is possible to simulate second order prototype elements by combining the two–pairs simulating first order elements, practical considerations dictate the use of second order two–pairs where possible, as described in section 4.3.3.

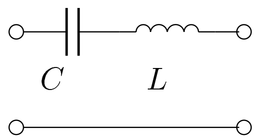
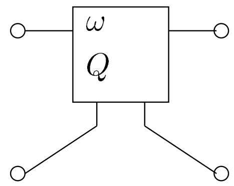
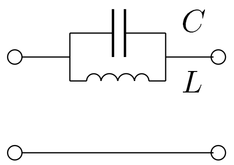
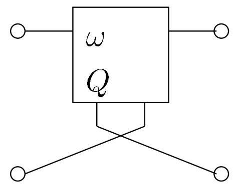
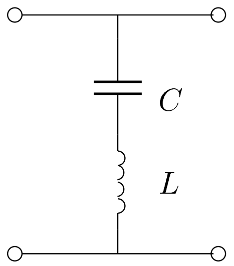
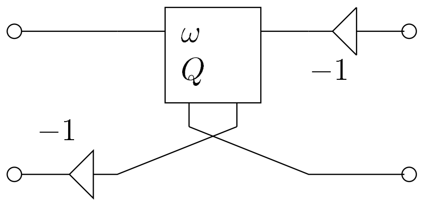
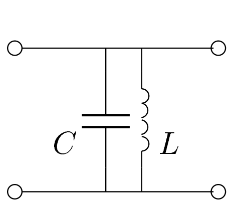
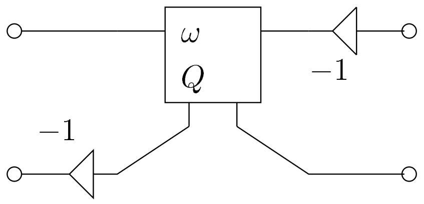
Prototype elements	complete Two–pair	Time constants
		$\omega = \sqrt{1/(LC)}$ $Q = 1/(2R)\sqrt{L/C}$
		$\omega = \sqrt{1/(LC)}$ $Q = 2R\sqrt{C/L}$
		$\omega = \sqrt{1/(LC)}$ $Q = 2/R\sqrt{L/C}$
		$\omega = \sqrt{1/(LC)}$ $Q = R/2\sqrt{C/L}$

Table 3.2: Second order prototype branches and corresponding two–pairs built from second order elementary two–pair

From the **S** matrices (3.16) and (3.14) we get the general Signal Flow Graph (SFG) for the first and second order two–pairs to be as shown in figure 3.5. The SFG is found from rewriting the two **S** matrices as follows

$$\begin{aligned} B_1 &= A_1 - h(s)(A_1 - A_2) \\ B_2 &= A_2 + h(s)(A_1 - A_2) \end{aligned} \tag{3.19}$$

where $h(s)$ is the transfer function generally associated with the relevant prototype elements, i.e.

$$h(s) \;=\; \begin{cases} \dfrac{1}{1 \,+\, s\tau} & \text{For first order two–pairs} \\ \dfrac{s\,\omega/Q}{s^2 \,+\, s\,\omega/Q \,+\, \omega^2} & \text{For second order two–pairs} \end{cases} \tag{3.20}$$

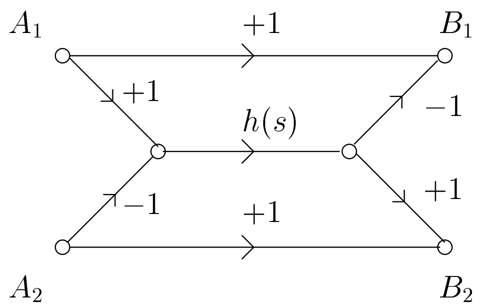


Figure 3.5: General Signal Flow Graph for simulation of simple LC structures

3.2.2 Simulation of LC Lattice structures

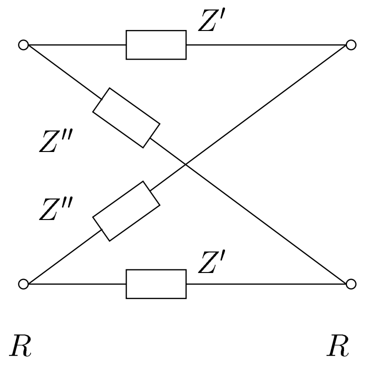


Figure 3.6: General Lattice section prototype

The last prototype treated is the Lattice section of first or second order. The Lattice section breaks with the unbalanced three–terminal ladder prototype structure (or, equivalently, with the restriction against coupled coils) traditionally used for integrated simulation topologies[4]. It should be noted that the term *lattice* refers to the shape of the prototype as drawn in figure 3.6; other uses of the term lattice do not necessarily refer to any related subject, e.g. the term "Lattice filter" which describes digital filters that are unrelated to LC filters with Lattice elements. Lattice sections are used in LC prototypes when the transfer fuction is required to be of a more general class than that obtainable from unbalanced ladders. It is possible to generate non minimum–phase transfer functions. Conventionally, Lattice sections are used in LC filters as pure phase equalisers, but it is possible to design circuits where the Lattice sections perform both amplitude and phase correction as described in e.g. [3.1, 3.7].

The general Lattice section is shown in figure 3.6 with the impedances Z' and Z'' both either first or second order of the structure shown in figure 3.7. The Signal Flow Graph of the two–pair simulating a Lattice section is shown in figure 3.8, as defined in [3.5, section VI A]. The two transfer functions S' and S'' are allpass functions defined by

$$\begin{aligned} S' &= \frac{Z' - R}{Z' + R} \\ S'' &= \frac{Z'' - R}{Z'' + R} \end{aligned} \tag{3.21}$$

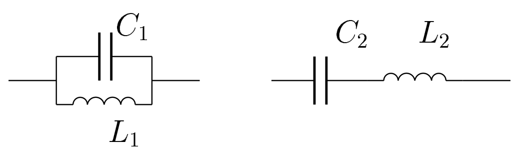


Figure 3.7: Z' and Z'' impedances for Lattice section

Restricting the choices for Z' and Z'' to first and second order impedances of

[4]In discrete Active–RC filters, coupled coil prototypes are not entirely unheard of, e.g. [3.6, 3.4]

the configuration shown in figure 3.7 we get the transfer functions S' and S'' to be

$$\begin{aligned} S' &= -\frac{s^2 - s/(C_1R) + 1/(C_1L_1)}{s^2 + s/(C_1R) + 1/(C_1L_1)} \\ S'' &= \frac{s^2 - sR/L_2 + 1/(C_2L_2)}{s^2 + sR/L_2 + 1/(C_2L_2)} \end{aligned} \tag{3.22}$$

For first order sections C_1 and L_2 have zero value (an open and a short circuit, respectively). For allpass prototype sections $Z'/R = R/Z''$, but for the more general case the Lattice section provides both amplitude and phase equalisation.

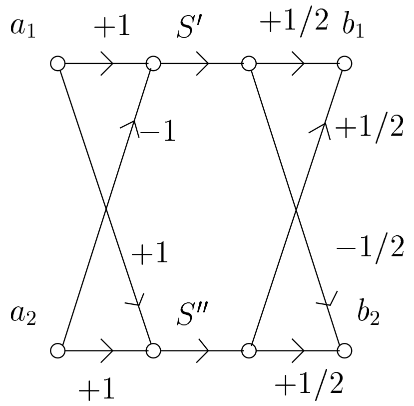


Figure 3.8: SFG for two–pair simulating general Lattice section

3.3 Discussion and conclusion

The general process of Wave Analysis leads to a simple synthesis procedure where each element in the prototype is simulated by a subcircuit where the parameters are dependent only on the component value(s) in the prototype element; in other words, the synthesis procedure does not involve any lengthy Wave Analysis of the complete prototype system. This makes the nominal design process for a Wave Active filter no more complicated than for a filter of conventional topology[5].

This chapter provides a simple introduction to ideal synthesis of WA filters by simulation of LCR prototypes. While the Wave state variables are alien to most filter designers, a systematic design process — where no analysis is performed — is made possible by the tables provided.

References

[3.1] B J Bennet. A new filter synthesis technique – the hourglass. *IEEE Transactions CAS*, 35(12):1469 – 1477, December 1988.

[3.2] C A Desoer and E S Kuh. *Basic Circuit Theory*. McCraw–Hill, 1969.

[3.3] H G Dimopoulos and A G Constantinides. Linear transformation active filters. *IEEE Transactions CAS*, 25(10):845 – 852, 1978.

[3.4] G Doblinger. High–order elliptical analog low–pass and band–pass filters with current controlled frequency responses. In *Proceedings of the International Symposium on Circuits and Systems*, pages 350 – 353. IEEE, 1982.

[3.5] A Fettweis. Wave digital filters: Theory and practice. *Proceedings of the IEEE*, 74(2), February 1986.

[3.6] M S Pieda and M M Silva. New lowpass and bandpass active filters derived from passive ladder prototypes. In *Proceedings of the International Symposium on Circuits and Systems*, pages 557–561. IEEE, 1980.

[3.7] J Tingleff and C Toumazou. Current mode wave active simulation of a linear phase LC filter using a lattice section. In H Dedieu, editor,

[5]Indeed, it might be argued that the process of writing up a "suitable" flow graph for the prototype — as part of the design of an SFG filter — is more complicated, since it involves considerations about the immediate surroundings for each element.

Proceedings of the European Conference on Circuit Theory and Design, pages 1373 – 1378. Elsevier Science Publishers, 1993.

Chapter 4

Current Mode Wave Active filter theory

While the ideal synthesis procedure is interesting as an intellectual exercise, the real merit of the CMWA topology (and of any other topology) is the performance of complete filter systems. Although measurement results are the only real indicators of actual quality, analysis based on models with varying levels of detail offer a very good indication of problem areas and the particular strengths and weaknesses of a topology.

In this chapter I consider a few points related to the performance of CMWA filters in the presence of errors in the realisation. Specifically, I will cover the effects of frequency independent errors and frequency dependent errors on the performance of CMWA filters based on first order two–pairs; for second order section based filters, I consider the Q factors for bandpass filters and the sensitivities of allpass Lattice simulations to implementation errors. Since it has unfortunately only been possible to spend a fraction of the necessary time on study of practical issues, a lot of important analysis has not been performed. The main points not covered (but important) are

- Distortion and noise — signal to noise ratio in general
- Tuning circuits.
- Analysis of errors in biquad based filters

This chapter opens with simple ideal synthesis of CMWA building blocks, followed by sections on practical issues involving first order section based filters and higher order section based filters. The most exhaustive treatment is of the first order based section filters for which several interesting properties are found.

4.1 Basic Current Mode Wave Active filter synthesis

While I have so far not mentioned the "mode" (Current or Voltage) of the implementation of Wave Active filters, there are real differences between Current and Voltage mode Wave Active filters, and I chose Current Mode because of the several advantages for integrated implementations of Wave Active filters.

The central frequency dependent operation (lossy integration or low–Q bandpass filtering) operates with both voltage and current state variables. This is inherent in Continuous Time integrators built from linear resistive and capacitive elements. The frequency independent operations are, however, inherently different in Voltage and Current mode implementations. Although equivalent in the ideal case, Voltage and Current Mode circuits for signal subtraction – duplication – summation have different practical properties making them suited for use in different practical implementations.

For a voltage mode implementation, the necessary addition and subtraction operations would most likely be performed using internal current variables (e.g. convert two input voltages to currents and sum the currents into a resistor to obtain a sum voltage). For low frequencies, this is performed very simply by a circuit with an op–amp and three resistors. For higher frequencies, the available op–amp gain might not be high enough, the parasitic capacitances would introduce errors and so forth. A Voltage mode structure without feedback (transconductances at the input, current summation into a resistor and a voltage output buffer) would suffer from matching problems equivalent to the λ introduced errors described by the constants K_1 and K_2 in section 4.3.1.

In a practical circuit, it is desirable to be able to tune out the various gain errors. It is shown below — for the Current Mode implementation — how a simple tuning of transconductance gain (which is needed in the circuit in any case) allows for compensation for a number of practical problems. The various classical Wave Active filters (all voltage mode) use plain resistors to produce RC time constants and to perform many of the frequency independent operations. In an integrated implementation, the inevitable need for tuning would make active–RC circuits highly unsuitable.

4.1.1 Current Mode two–pair implementations

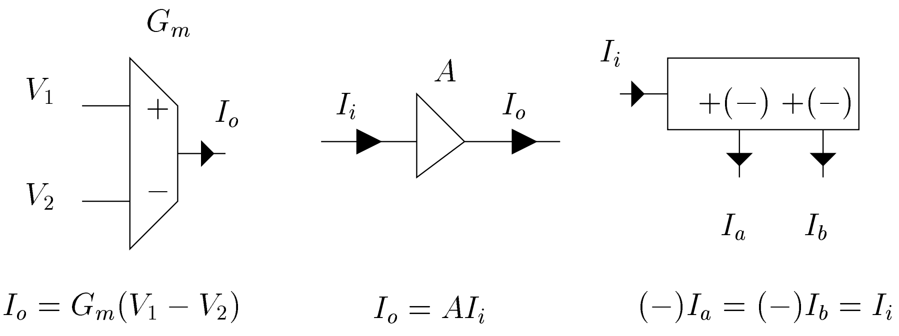


Figure 4.1: Current Mode building blocks; OTA, current amplifier and current duplicator

Based on the equations (3.19) I arrive at the circuit implementations proper.

The building blocks are: the Operational Transconductance Amplifier, the Current Duplicator and the Current Amplifier. The OTA is a conventional dual–input single–output amplifier, the current duplicator is a dual–output current mirror with optional inversion. The building blocks are shown in figure 4.1.

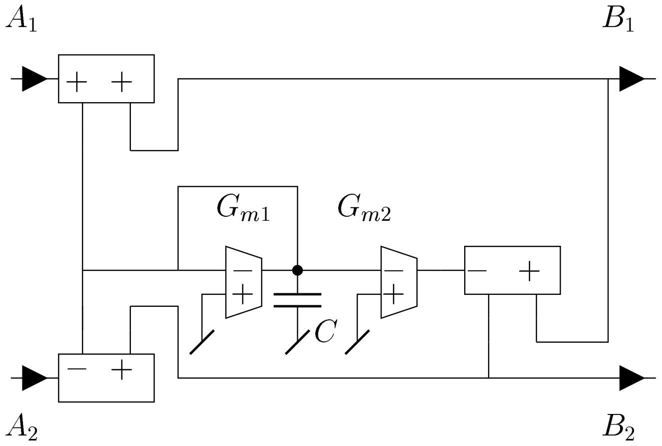


Figure 4.2: CMWA first order elementary two–pair

Using currents for the variables $A_{1/2}$ and $B_{1/2}$, current duplicators are used to implement the duplication at the input nodes and current summation is used to implement the summing at the output nodes. With the Current Mode building blocks, the first order two–pair can be implemented as shown in figure 4.2. Note that the OTA generating the output from the integration could be a dual output amplifier feeding the $B_{1/2}$ outputs directly, but for the CMOS implementation described later this was not chosen. Assuming ideal building blocks, the transfer functions are as follows

$$\begin{aligned} B_2/A_1 &= B_1/A_2 = \frac{G_{m2}}{G_{m1} + sC} \\ B_2/A_2 &= B_1/A_1 = 1 - \frac{G_{m2}}{G_{m1} + sC} \end{aligned} \tag{4.1}$$

Assuming $G_{m1} = G_{m2} = G_m$ these equations reduce to (3.14) with the time constant being $\tau = C/G_m$. If inverters are needed when combining the two–pairs into filters, they are simply implemented by switching the outputs of the current duplicator at the A_2 input (since the inverter always appears at an A_2 input).

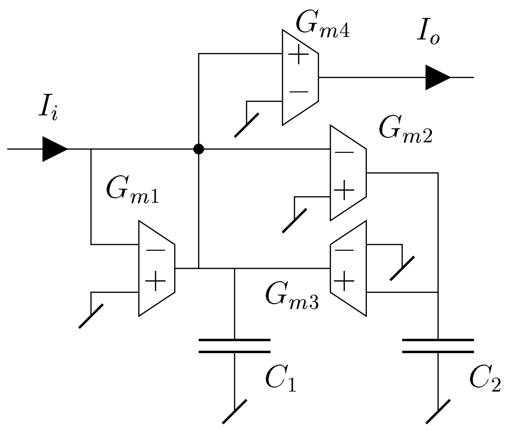


Figure 4.3: Bandpass biquad section with current input/output

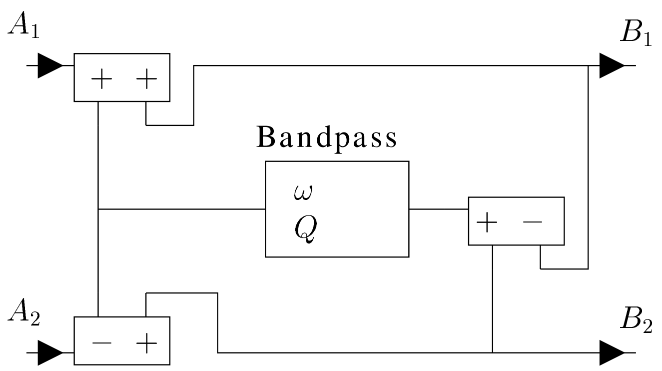


Figure 4.4: CMWA second order elementary two–pair

For the bandpass biquad I use a gyrator–C simulation of a resistively loaded parallel resonance circuit connected in shunt. The OTA–C circuit is shown in figure 4.3. The transfer function is

$$\frac{I_o}{I_i} = \frac{G_{m4}C_2 s}{C_1 C_2 s^2 + G_{m1}C_2 s + G_{m2}G_{m3}} \tag{4.2}$$

Assuming all transconductance values equal to G_m, the characteristics are

$$\begin{aligned} \omega &= G_m \frac{1}{\sqrt{C_1 C_2}} \\ Q &= \sqrt{\frac{C_1}{C_2}} \end{aligned} \tag{4.3}$$

Note that while this biquad has a higher capacitance spread than some other structures, all transconductance values are equal which simplifies the tuning process and improves matching. Since the only difference between the first and second order two–pairs is the transfer function $h(s)$, the circuits are much the same, with the bandpass biquad in figure 4.3 inserted in the box in figure 4.4.

To implement the Lattice section simulation, a circuit is derived from the SFG in much the same way as was the case for the plain ladder elements simulations. The resulting structure, shown in figure 4.5, simply provides the sum and difference as inputs to the two allpass sections $-S'$ and S''; the outputs are then combined to form the two–pair output.

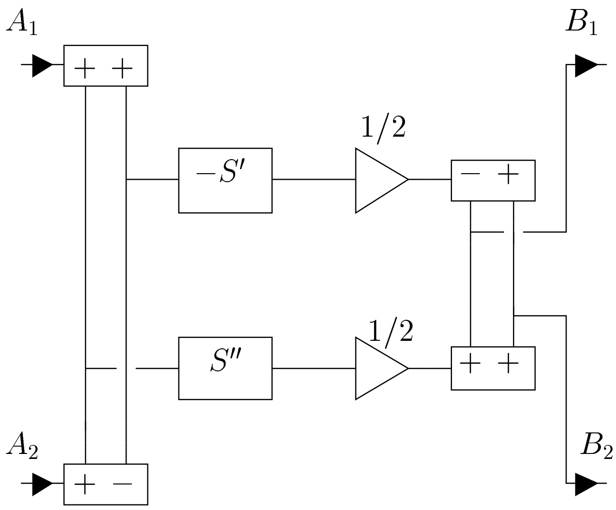


Figure 4.5: CMWA Lattice section simulation two–pair

I consider the second order Lattice to be the most interesting structure, so

I only give the Current Mode allpass biquad to be used for the $-S'$ and S'' sections. By taking a general two–integrator loop and putting input current into the relevant nodes and constructing the output from the difference between two node voltages I find the allpass biquad as shown in figure 4.6. The transfer function is

$$\frac{I_o}{I_i} = \frac{G_{m5}(C_1C_2s^2 - G_{m2}C_1s + G_{m2}(G_{m3}+G_{m4}-G_{m1}))}{G_{m4}C_1C_2s^2 + G_{m2}G_{m3}C_1s + G_{m1}G_{m2}G_{m3}} \tag{4.4}$$

which, assuming equal values for transconductance gain, gives the characteristics as follows

$$\begin{aligned} \omega &= G_m\frac{1}{\sqrt{C_1C_2}} \\ Q &= \sqrt{\frac{C_2}{C_1}} \end{aligned} \tag{4.5}$$

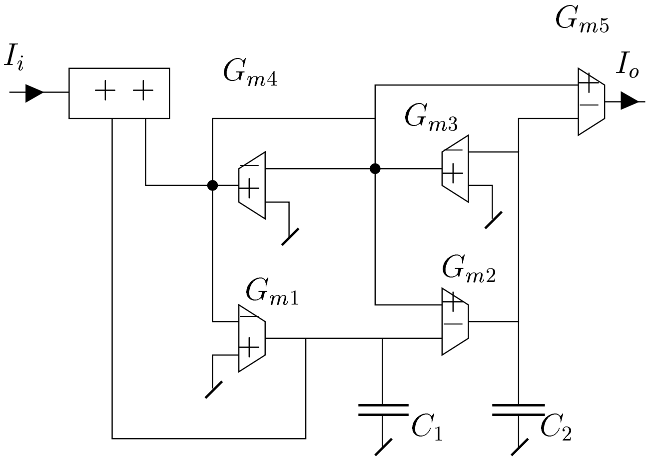


Figure 4.6: Allpass biquad section with current input/output

4.2 General sensitivity considerations

The often repeated claim that LCR prototypes (more specifically lossless ladders terminated by two resistances) have low sensitivity is based on the fact the passband transmission maxima are zero points for the first order sensitivity to component value changes. If a large number of zeros are placed in the passband, the maximum sensitivity cannot be "too large". In the stopband(s), the ladder nature of the filter ensures that signals are attenuated, no matter what the actual component values are. Slightly more stringent versions of this argument are given in [4.2, 4.5]. Since the CMWA topology has exactly one reactive component for each reactive component in the prototype[1], the sensitivity to changes in integration capacitances is the same as the sensitivity of the prototype to changes in reactive component values.

Unfortunately, the sensitivity of LCR prototypes to resistive losses in the reactive components is not low at all. Thus, as described in e.g. [4.6], any error in a simulation of an LCR prototype which is *not* simply equivalent to a change in prototype reactive component value indicates a potential problem. In the specific case of Wave Active filters, the equivalent of resistive loss is deviation from unity gain at maximum points or larger than zero gain at minimum points (as described in [4.2]).

4.3 Errors in first order section based filters

Since the first order section based work is by far the older, more theoretical work has been done. Since an integrated filter has been built, the comparison between theory and practice has been possible; as we shall se later, the measurements from the integrated filter fully supports the relevant conclusions from the theory.

[1]Each τ value in table 3.1 is directly proportional to a component value and define one capacitance value; the $Q - \omega$ equations in table 3.2 can be written to give expressions for the capacitances in the biquad in figure 4.3 in a similar manner, i.e. each capacitor value depends on one prototype component value only

4.3.1 Modelling of errors in building blocks

Since the following sections deal with filters based on first order two–pairs, the macromodels used are based on the simulation results for the CMOS implementation described in 5.2. The only point which is not obvious is that the amplifiers are assumed to have infinite bandwidth. This is only the case for very simple structures (in the case of the filter described here, the OTA is a long tailed pair) although some OTAs with high quality and very high bandwidth have been described, e.g. [4.3]. Because of the quality requirements set for the current duplicators, the rolloff frequencies are much lower than that of the OTA.

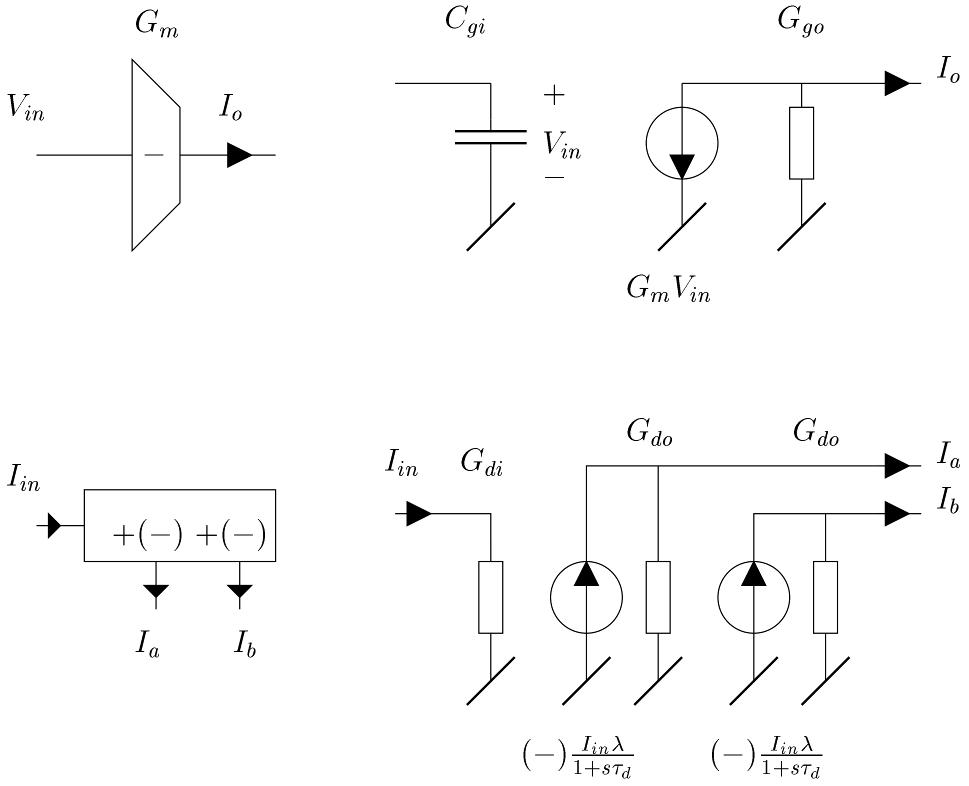


Figure 4.7: Building blocks for first order two–pairs with imperfections

The two types of building blocks are show in figure 4.7 with the chosen imperfections. The transfer matrix of the two-pair is built from two contributions: the transfer that is approximately 1, and the transfer that is approximately

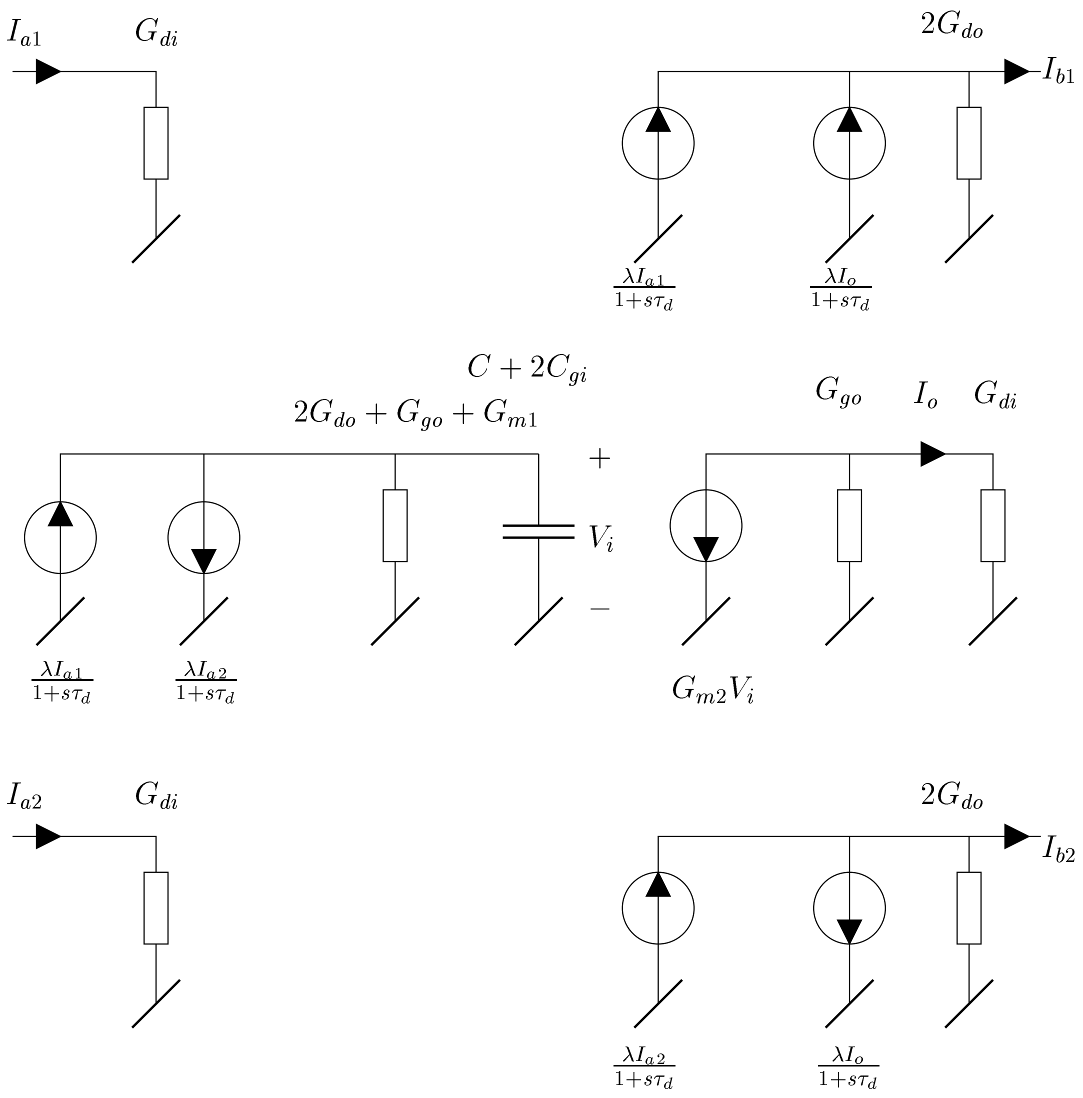


Figure 4.8: First order two–pair with imperfections

$1/(1 + s\tau)$. The transfer matrix is formed in the following way:

$$\mathbf{S} = \begin{bmatrix} \alpha - \beta & \beta \\ \beta & \alpha - \beta \end{bmatrix} \tag{4.6}$$

Observing the total equivalent diagram for a two–pair in figure 4.8, α and β are computed to be

$$\alpha = \frac{K_1}{1 + s\tau_d} \tag{4.7}$$

$$\beta = \frac{K_2}{(1 + s\tau')(1 + s\tau_d)^2} \tag{4.8}$$

with the constants K_1, K_2 and τ' defined as

$$K_1 = \frac{G_{di}\lambda}{G_{di} + 2G_{do}} \approx 1 \tag{4.9}$$

$$K_2 = \frac{G_{di}^2 G_{m2}\lambda^2}{(G_{di} + 2G_{do})(G_{di} + G_{go})(2G_{do} + 2G_{go} + G_{m1})} \approx 1 \tag{4.10}$$

$$\tau' = \frac{C + 2C_{gi}}{2G_{do} + G_{go} + G_{m1}} \approx \frac{C}{G_{m1}} \tag{4.11}$$

In the following I ignore the change in the main time constant, since it does not cause any changes in the form of the transfer function (only in the transfer function coefficients). If a well characterised process is used, it should be feasible to modify the integration capacitor value to make the time constant very nearly equal to the desired value. (The limiting factor for time constant precision is the fact that the absolute value of C_{gi} changes with the tuning of G_m, and so extremely high precision is not obtainable.)

4.3.2 Biquad simulations using first order two–pairs

Although the general aim is to produce high order filters, the behaviour of biquad simulations provide some important clues to the behaviour of higher order filters. Furthermore, the complexity of the equations prove to be excessive for any circuit of much higher order.

In figure 4.9 I give the LC–ladder prototype for a low–pass biquad and the Wave Active equivalent. The transfer function I_o/I_i is computed to be

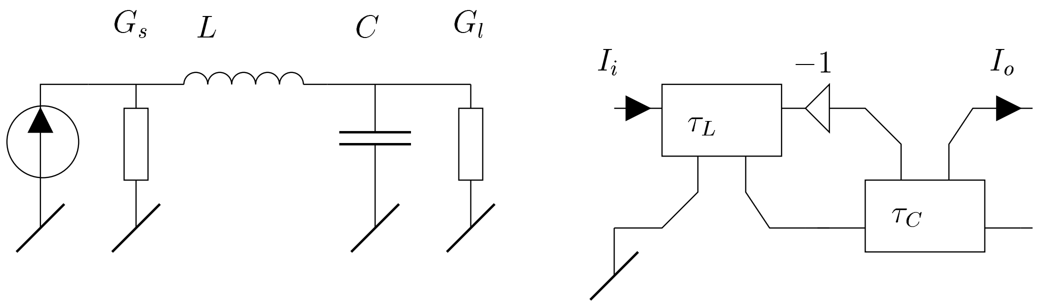


Figure 4.9: Lowpass LCR biquad and first order two–pair simulation

$$
\begin{aligned}
\frac{I_o}{I_i} = K_2^2/ \Big(&1 + {K_1}^2 - 2K_1K_2 + {K_2}^2 \\
&+ s \Big(\tau_C + {K_1}^2\tau_C - K_1K_2\tau_C + 4\tau_d + 2{K_1}^2\tau_d - 2K_1K_2\tau_d \\
&\quad +\tau_L + {K_1}^2\tau_L - K_1K_2\tau_L\Big) \\
&+ s^2 \Big(4\tau_C\tau_d + 2{K_1}^2\tau_C\tau_d - K_1K_2\tau_C\tau_d + 6{\tau_d}^2 + {K_1}^2{\tau_d}^2 \\
&\quad +\tau_C\tau_L + {K_1}^2\tau_C\tau_L + 4\tau_d\tau_L + 2{K_1}^2\tau_d\tau_L - K_1K_2\tau_d\tau_L\Big) \\
&+ s^3 \Big(6\tau_C{\tau_d}^2 + {K_1}^2\tau_C{\tau_d}^2 + 4{\tau_d}^3 + 4\tau_C\tau_d\tau_L \\
&\quad + 2{K_1}^2\tau_C\tau_d\tau_L + 6{\tau_d}^2\tau_L + {K_1}^2{\tau_d}^2\tau_L\Big) \\
&+ s^4 \Big(4\tau_C{\tau_d}^3 + {\tau_d}^4 + 6\tau_C{\tau_d}^2\tau_L + {K_1}^2\tau_C{\tau_d}^2\tau_L + 4{\tau_d}^3\tau_L\Big) \\
&+ s^5 \Big(\tau_C{\tau_d}^4 + 4\tau_C{\tau_d}^3\tau_L + {\tau_d}^4\tau_L\Big) + s^6\tau_C{\tau_d}^4\tau_L\Big)
\end{aligned}
\tag{4.12}
$$

Note that this circuit remains stable for all reasonable values of K_1, K_2 and τ_d. This is revealed by the positive sign of all coefficients. (The "reasonable" above represents the assumption that the K values do not deviate too much from 1.)

I examine the dependency of ω and Q on the frequency performance of the building blocks by setting the DC errors to zero ($K_1 = K_2 = 1$) and varying τ_d. I compute the first order Taylor series approximation to the true $\omega(\tau_d)$ and $Q(\tau_d)$ functions by computing the derivative value for $\tau_d = 0$, as outlined in section B.2.

$$\omega = \frac{1}{\sqrt{2}\sqrt{\tau_C\tau_L}} - \tau_d\frac{(\tau_C+\tau_L)}{\sqrt{8}\tau_C{}^{\frac{3}{2}}\tau_L{}^{\frac{3}{2}}} + \mathrm{O}(\tau_\mathrm{d}^2) \tag{4.13}$$

$$Q = \frac{\sqrt{2}\sqrt{\tau_C\tau_L}}{\tau_C+\tau_L} + \tau_d\frac{(\tau_C{}^2+\tau_L{}^2)}{\sqrt{2}\tau_C{}^{\frac{5}{2}}\sqrt{\tau_L}+2\sqrt{2}\tau_C{}^{\frac{3}{2}}\tau_L{}^{\frac{3}{2}}+\sqrt{2}\sqrt{\tau_C}\tau_L{}^{\frac{5}{2}}} + \mathrm{O}(\tau_\mathrm{d}^2) \tag{4.14}$$

Naming the constant terms in these expressions ω_0 and Q_0, i.e.

$$\omega_0 = \frac{1}{\sqrt{2}\sqrt{\tau_C\tau_L}} \tag{4.15}$$

$$Q_0 = \frac{\sqrt{2}\sqrt{\tau_C\tau_L}}{\tau_C+\tau_L} \tag{4.16}$$

and using the ratio between the cut–off frequency and the duplicator pole as time constant variable, $\omega_0\tau_d$, I arrive at the following expressions

$$\omega = \omega_0(1-\frac{1}{Q_0}(\omega_0\tau_d)) + \mathrm{O}(\tau_\mathrm{d}^2) \tag{4.17}$$

$$Q = Q_0 + \frac{\tau_C^2+\tau_L^2}{(\tau_C+\tau_L)^2}(\omega_0\tau_d) + \mathrm{O}(\tau_\mathrm{d}^2) \tag{4.18}$$

Setting the duplicator parasitic pole to infinity, I get the errors caused by the resistive parasitics. The transfer function value at DC is indicative of the gain error below the cutoff frequency of the filter. This result is reached simply by setting $s = 0$ in (4.12)

$$\left.\frac{I_o}{I_i}\right|_{s=0} = \frac{K_2{}^2}{1+K_1{}^2-2K_1K_2+K_2{}^2} \tag{4.19}$$

The main pole of the filter gets shifted slightly by the DC errors, as indicated by the expressions below (these expressions are exact)

$$\omega = \frac{\sqrt{1+K_1{}^2-2K_1K_2+K_2{}^2}}{\sqrt{\tau_C\tau_L+K_1{}^2\tau_C\tau_L}} \tag{4.20}$$

$$Q = \frac{\sqrt{1+K_1{}^2-2K_1K_2+K_2{}^2}\sqrt{\tau_C\tau_L+K_1{}^2\tau_C\tau_L}}{\left(1+K_1{}^2-K_1K_2\right)(\tau_C+\tau_L)} \tag{4.21}$$

One very important result comes from equations (4.18) and (4.21): the process of tuning amplifier gain, G_{m1} and G_{m2}, may compensate for high frequency errors in the building blocks. Whereas the effect of the HF pole is to increase the Q, variations of the gain constants K_1 and K_2 can either increase or decrease the Q.

4.3.3 High frequency problems

Apart from the precision problems discussed above, there are some cases where Wave Active simulations of LC–ladder filters exhibit peaks in the frequency response, or even oscillate. These are the problems alluded to in the MWSCAS–92 paper. In the literature, I have only found a reference in one paper, reference [4.4] (no "physical interpretation" was offered).

For this reason, filters with finite transmission zeros are not attempted. For a 6th order bandpass filter with finite transmission zeros, the simple prototype (shunt parallel resonator followed by two parallel resonators in series followed by a parallel resonator in shunt), the CMWA simulation based on first order two–pairs exhibit oscillation. A minimum–L prototype exhibits only a severe change in passband shape. Both prototypes have redundant structures (i.e. capacitor loops) which seem to account for the problems, but they have different actual structures, indicating that the severity of the problem is dependent on prototype topology. The relation between topology (ideal transfer function) and these problems is one of the most annoyingly unsolved problems for first–order based CMWA filters. I suspect that second order two–pairs would cure this problem, but I have not looked into that (I would prefer to find the actual reason first).

It should be noted that there is a strong indicator of high frequency problems: the presence of a loop with an ideal gain of 1 at infinity. The loop in a lowpass biquad, figure 4.9, has a gain of -1 at infinity, which is entirely safe. One indicator of (in)stability is the signs of the coefficients in the denominator polynomial; if all coefficients have the same sign, it is certain that no poles are located in the right half–plane.

The problem is simply illustrated by the simulation of two parallel capacitors. Figure 4.10 shows the prototype, Wave Active simulation and the signal flow graph of the Wave Active simulation. The transfer functions s^a_{11} — s^b_{22} are formed as described above. Using Mason's formula, I get the transfer function to be

$$\frac{b_2}{a_1} = \frac{s^a_{12}\, s^b_{21}}{1 - s^a_{22} s^b_{11}} \tag{4.22}$$

which, given the ideal transfer functions below, simplifies as follows:

$$\begin{aligned}
s^a_{11} &= s^a_{22} = \frac{s\tau_a}{1 + s\tau_a}, \quad s^a_{21} = s^a_{12} = \frac{1}{1 + s\tau_a} \\
s^b_{11} &= s^b_{22} = \frac{s\tau_b}{1 + s\tau_b}, \quad s^a_{12} = s^b_{12} = \frac{1}{1 + s\tau_b} && (4.23) \\
\frac{b_2}{a_1} &= \frac{1}{1 + s(\tau_a + \tau_b)} && (4.24)
\end{aligned}$$

The ideal expressions conceal the fact that this circuit has a possible instability at infinite frequency. At infinite frequency, the capacitors act as short circuits, and thus a current of any magnitude can circulate in the loop formed by the two capacitors. This is mirrored in the SFG of the Wave Active simulation in the loop $s^a_{22}s^b_{11}$ which, ideally, has a gain of 1 at infinite frequency. When building the Wave Active circuit, there are no active components with a gain of 1 at infinite frequency, so the pole at infinity has to move and/or split into several poles.

Setting both the s_{11} and s_{12} functions to have a first order roll-off at $1/\tau_d$ (assuming as always $\tau_d \ll \tau$), I get (with s^b similarly modified):

$$s^a_{11} = s^a_{22} = \frac{s\tau_a}{(1 + s\tau_a)(1 + s\tau_d)}$$

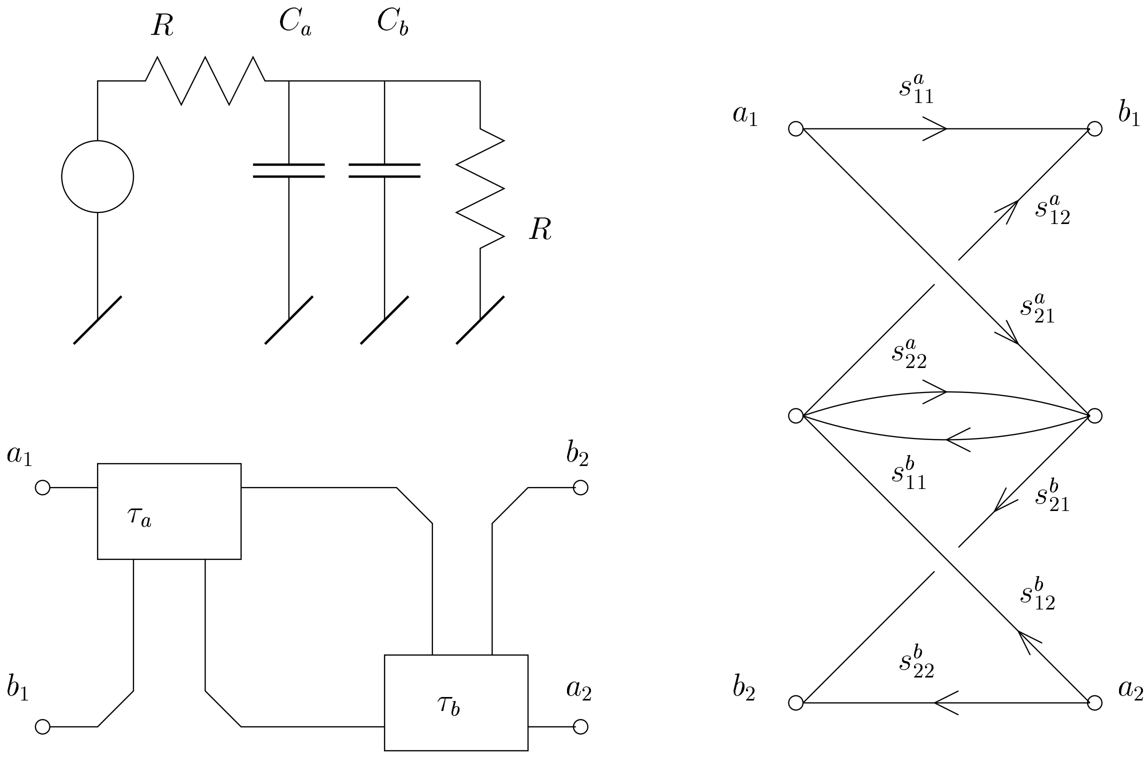


Figure 4.10: Parallel C circuit. Prototype, Wave Active simulation: schematic and SFG

$$s_{21}^a = s_{12}^a = \frac{1}{(1 + s\tau_a)(1 + s\tau_d)} \tag{4.25}$$

$$\frac{b_2}{a_1} = 1/\Big(1 + s\left(\tau_a + \tau_b + 2\tau_d\right) + s^2\left(2\tau_a\tau_d + 2\tau_b\tau_d + {\tau_d}^2\right) + s^3\left(2\tau_a\tau_b\tau_d + \tau_a{\tau_d}^2 + \tau_b{\tau_d}^2\right) + s^4\tau_a\tau_b{\tau_d}^2\Big) \tag{4.26}$$

When setting $\tau_a = \tau_b = \tau/2$ and finding the poles of transfer function (4.26) four solutions are found:

$$s = -\frac{1}{\tau} \pm \frac{\sqrt{4/\tau^2 - 8/(\tau\tau_d)}}{2} \tag{4.27}$$

$$s = -\frac{1}{\tau} - \frac{1}{\tau_d} \pm \frac{\sqrt{4/\tau^2 + 4/{\tau_d}^2}}{2} \tag{4.28}$$

The first two solutions are obviously problematic since they have very high Q at a frequency $\omega \approx \sqrt{2/\tau_d}$, and will cause a sharp peak in the response curve. The two last solutions are the slightly distorted designed solution, $s \approx -1/\tau$, and a real pole at high frequency, $s \approx -2/\tau_d$, which is not significant.

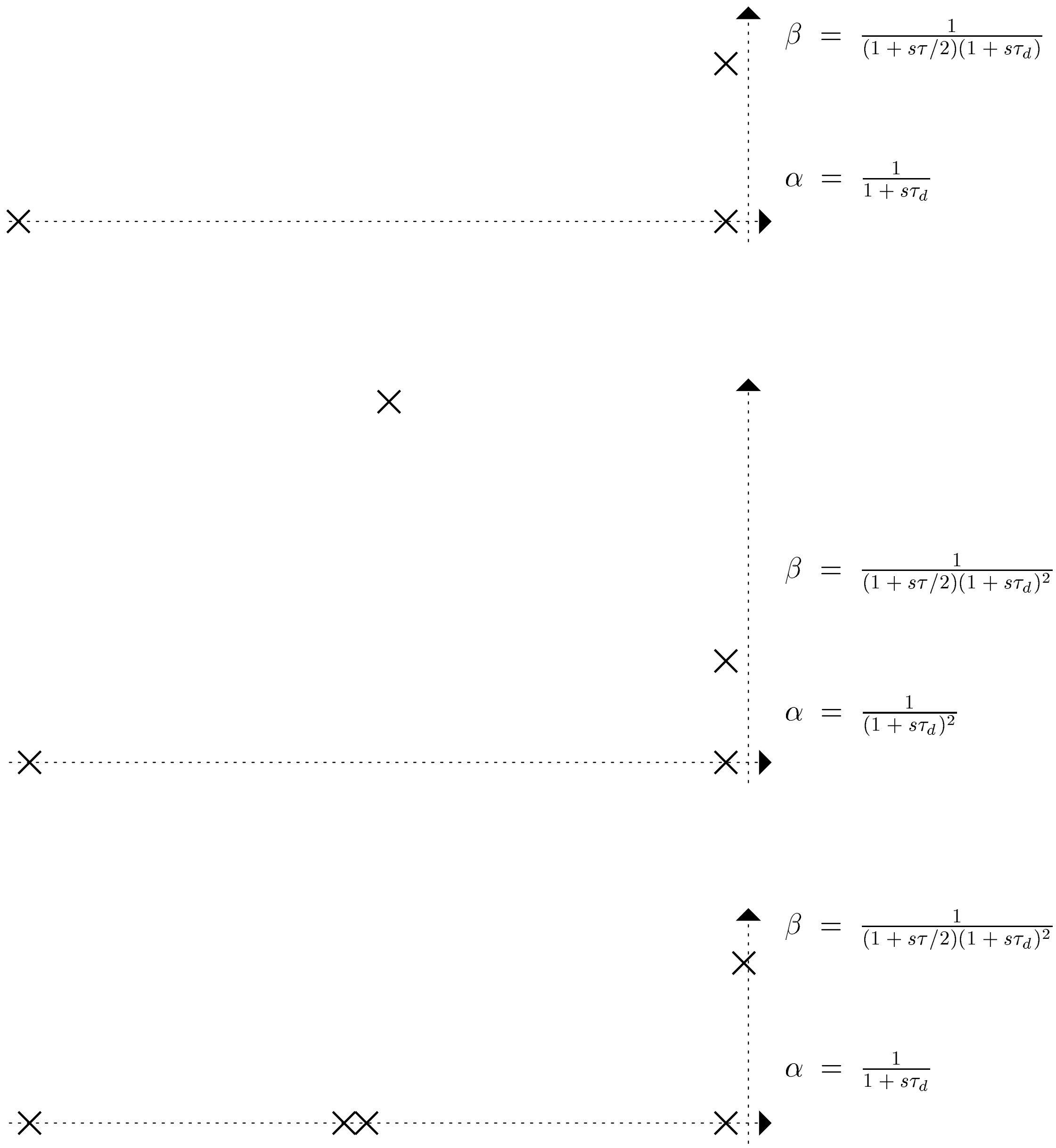


Figure 4.11: Pole patterns for parallel C simulation for various imperfection approximations

The symbolic solution above only looks nice and simple for $\tau_a = \tau_b$. For every other case the symbolic solutions are much larger (the symbolic output of the maths program is less than 10 lines for the solutions above, and more than

1000 lines for the more general solution). Numerical experiments show that the Q of the main parasitic pole pair is at a maximum for $\tau_a = \tau_b$, but nothing changes radically by the change of τ values.

Changing assumptions about the nature of the parasitics changes the number of low–Q poles and their position, but not the main parasitic poles. In figure 4.11 the poles for a number of imperfection assumptions are shown (the top half of the left half–plane only is shown), with α and β as used in (4.6). The fact that the high–Q parasitic poles are in practically identical positions indicate that the problem is not confined to a specific implementation method or to a specific set of imperfection assumptions.

The symbolic and numerical results here share one fault: they do not indicate what the cause of the problem is. Thus, it is necessary to perform an analysis of each new filter in order to be certain that there are no problems.

4.4 Practical considerations for biquad based filters

While biquad based sections (both simulations of second order prototype sections and the use of two allpass biquads to simulate second order Lattice sections) have not been treated as thoroughly as the earlier filter type, some results have been reached. First, the quality factors of the poles in the biquads are shown to be (much) smaller than those of the actual transfer function and secondly, the amplitude sensitivity of a phase equaliser built from the redundant structures is shown to be smaller than for a trivially equivalent cascade structure. Both of these results are found through numerical computations on specific examples and are thus not claimed to be generally valid, but do give an indication of the practical qualities of CMWA filters based on higher order sections. It should be noted that the first property is generally valid for Wave filters, be they digital or analogue and independent of the implementation, and that the second is probably also generally valid.

4.4.1 On the Q values of biquads in bandpass filters

One interesting aspect of CMWA filters based on biquads is that the Q values of the biquads tend to be low, lower than the Q values of the transfer function. The only reference in the literature to this effect [4.9] is quite brief, so I include a series of computations here. One reason that this is an interesting question is that the sensitivity of Q in biquads can be proportional to Q^2; it will be shown later that the ratio between maximum Q in the transfer function and maximum biquad Q in a CMWA simulation may exceed 10 — leading to a dramatic benefit for the CMWA simulation compared to cascade realisations.

The computations performed are numerical computations on filters derived from lowpass prototypes from a table [4.8] for which tabulated values of transfer function poles are taken[2]. All prototypes are designated by their corresponding lowpass equivalent, i.e. "Txxyy" where "T" means Chebyshev characteristic, "xx" is the filter order and "yy" indicates the passband ripple (the larger the number the larger the ripple). The experiment involves taking a lowpass prototype and generating a bandpass prototype by the trivial lowpass to bandpass frequency transform (for centre frequency 1):

$$s = \sigma + j\omega = \hat{Q}\left(\frac{1}{\tilde{s}} + \tilde{s}\right) \tag{4.29}$$

$$\tilde{\omega}_{\pm} = \sqrt{\left(\frac{\omega}{2\hat{Q}}\right)^2 + 1} \pm \frac{\omega}{2\hat{Q}} \tag{4.30}$$

where (4.29) defines the transform from bandpass complex frequency $\tilde{s}$ to lowpass complex frequency s and (4.30) defines the reverse transform from a

[2]It is possible to derive closed form expressions for all the values found here. Given that tabulated values are available, the trouble of working out exact solutions was avoided

point on the imaginary axis in the lowpass frequency domain ω to two points on the imaginary axis in the bandpass frequency domain, $\tilde{\omega}_-$ and $\tilde{\omega}_+$, with $\tilde{\omega}_- < 1$ and $\tilde{\omega}_- \tilde{\omega}_+ = 1$. The inverse of the relative bandwidth is named $\hat{Q}$, defined from the transform of the cutoff frequency in the prototype domain, ω_p, as

$$\hat{Q} \;=\; \frac{1}{\tilde{\omega}_{p+} - \tilde{\omega}_{p-}} \tag{4.31}$$

The advantage of this frequency transform is that prototype components in the lowpass filter is transformed into simple component networks in the bandpass filter, the two transforms used are shown in table 4.1.

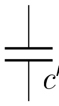
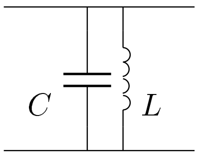
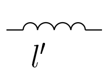
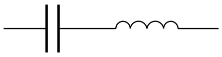
Lowpass element	bandpass equivalent	Component values
 c'	 C L	$C = 1/L = \hat{Q}c'$
 l'	 C L	$L = 1/C = \hat{Q}l'$

Table 4.1: Lowpass to bandpass transform for elements, centre frequency 1

It was found that the maximum Q of the transfer function was approximately proportional to $\hat{Q}$, and for this reason, a fixed value of $\hat{Q} = 10$ was used (the proportionality was correct down to a few percent error from $3 < \hat{Q}$ and up). The maximum Q value in the bandpass transfer function is denoted $Q^H_{\max}$, the maximum Q value in a biquad in a CMWA simulation is denoted $Q^B_{\max}$. From the table 3.2 it is found that the maximum Q value for a biquad in a CMWA simulation of a bandpass filter is given by the prototype component values and $\hat{Q}$ as follows (assuming Wave Analysis R value of 1, with x_i the normalised component values):

$$Q^B_{\max} \;=\; \max_i \left\{ \frac{\hat{Q} x_i}{2} \right\} \tag{4.32}$$

Lowpass design	Ripple, dB	$Q^H_{\max}$	$Q^B_{\max}$
T0301	0.0004	7.1	3.2
T0302	0.0017	9.1	3.9
T0303	0.0039	10.6	4.4
T0305	0.0109	12.8	4.9
T0308	0.0279	15.5	5.3
T0310	0.0436	17.1	5.5
T0315	0.0988	20.6	5.7
T0320	0.1773	23.8	5.9
T0325	0.2803	26.9	6.7

Table 4.2: Q values for fixed filter order and varied passband ripple, $\hat{Q} = 10$

The first experiment involves taking a third order lowpass filter with Chebyshev characteristic and varying the passband ripple. (Increasing the passband ripple increases the slope of the transition band by increasing the $Q^H_{\max}$ value.) For the prototype lowpass designs `T0301` to `T0325` (defined by the passband ripple values given in the table), the Q values are computed and given in table 4.2.

Lowpass design	$Q^H_{\max}$	$Q^B_{\max}$
T0315	20.6	5.7
T0415b	37.8	8.8
T0515	59.9	9.9
T0615b	87.1	10.3
T0715	119.1	10.5
T0815b	156.1	10.8
T0915	198.0	11.0
T1015b	244.9	11.1
T1115	296.7	11.2

Table 4.3: Q values for varying filter order and fixed passband ripple, $\hat{Q} = 10$

The second experiment involves taking a fixed passband ripple and increasing the filter order. For the prototype designs `T0315` to `T1115` the results are as tabulated in table 4.3. While it is perhaps not very likely that anyone would want to build a 22nd order filter, the results for realistic filter orders (e.g. 8th order bandpass) are still very convincing.

4.4.2 Sensitivity of complete Lattice simulation compared to cascade equivalent

For the case where the LC Lattice is an all–pass structure, the two reflectance transfer functions of the Wave Active simulation (b_1/a_1 and b_2/a_2) are ideally zero, since $S' = -S''$. Thus, ideally, a series of all–pass Lattice sections connected between an amplitude filter and the load resistor is simulated simply by a cascade of all–pass circuits. We suspect that the actual variation of performance, given variations in parameter values, is smaller for the full Wave Active simulation than for the ideally equivalent cascade realisation. The full Wave Active simulation, like the LC prototype, has full interaction between all elements/sections, a fact which has been used to explain the low sensitivity of LC prototypes.

To test the idea that the redundancy of providing two identical subblocks provide less final variability, we simulated a 9th order phase equaliser. The phase equaliser consists of one first order section[3] and four second order sections, with σ – Q/ω values as given in table 4.4 (the σ value is the real zero/pole in the first order allpass section). The amplitude filter is a 7th order Chebyshev characteristic lowpass filter with 0.25 dB passband amplitude ripple. The group delay equaliser was designed with a computer program to give approximate equi–ripple approximation to constant group delay; with four peaks at the maximum group delay of 28.8 s and four lower extrema at 25.2 s in the frequency band $[0, 1.2]$ rad/s for a cutoff frequency of 1 rad/s. The Wave Active phase equaliser consists of five generic Lattice simulation blocks, with the first being first order and the last four being second order. The simple cascade realisation connects one first order all–pass circuit and four second order biquads (identical to the allpass sections used in the Lattice simulation).

[3]Implementations of first order Lattice sections have not been touched on in this thesis; the first order section given in [4.10] rely on a virtual ground output point, and are not considered really feasible.

Section	Characteristics
1	$\sigma = 0.77556$
2	$\omega = 0.32280$ $Q = 0.54512$
3	$\omega = 0.98569$ $Q = 0.41961$
4	$\omega = 0.50606$ $Q = 1.2773$
5	$\omega = 0.83286$ $Q = 2.5566$

Table 4.4: Characteristics of phase equaliser sections

The simulation used to test the sensitivity is Monte Carlo analysis, with $\pm 1\%$ variation in all primary values (G_m, A, C, ...) for the phase equalisers (but not in the amplitude filter). The mean values of group delay peak–to–peak variation are 4.01 and 3.96 seconds, for the CMWA and cascade implementation respectively. The SD[4] values are 0.227 and 0.185 respectively. For the amplitude, the mean values of the variation are 0.567 and 0.665 dB respectively, while the SD values are 0.134 and 0.191. (Note that the unvarying amplitude variation of 0.25 dB from the amplitude filter is included in these figures.) It is observed that the variation in amplitude for the cascade realisation is larger than that for the full Wave Active realisation. The variation in group delay is slightly larger for the Wave Active realisation, but not alarmingly so. The interesting fact is that the gain variation is lower although more circuits are used, indicating that the "connectedness" — i.e. the influence of all elements on all transfer function poles — gives a real benefit. The observation that the gain sensitivity is smaller and the group delay sensitivity slightly larger for "ladder–type" Lattice simulations is also made in references [4.1, 4.7].

4.5 Discussion and conclusion

The various structures shown here demonstrate the ease with which the frequency independent operations are implemented with Current Mode building

[4] Standard Deviation. The square root of the average of the square of the difference between the values and the mean value

blocks, fully justifying the use of Current Mode for integrated Wave Active filters. All the frequency dependent operations are implemented with structures which have grounded capacitors only, have equal valued transconductance amplifiers and have no high impedance nodes. All time constants (in the first order based structures) or all centre frequencies (in the biquad based structures) are proportional to the transconductance value. The ratios between time constants or the quality factors are independent of the transconductance value. These facts lead to the general fact that the filters are frequency scalable by simple transconductance value tuning where the denormalisation frequency is simply proportional to the transconductance value.

For first order sections the effects of building block errors has been shown to be quite serious for some prototype structures — seemingly prototypes which exhibit instability at infinite frequency — although no conclusion has been reached as to the cause and possible cure for this. For structures that do not exhibit fatal errors, such as polynomial filters, the effects (in the passband) of high frequency limits have been shown to be correctable by amplifier gain tuning The ability to compensate for amplifier phase errors with gain tuning is believed to be unique to first order based CMWA filters.

For second order sections, two simple facts have been demonstrated in simulation of simple examples. Firstly, the maximum Q values for the biquads used in a bandpass filter simulation is dramatically lower than the maximum Q value in the transfer function; secondly, the amplitude variation in a phase equaliser built from the full Lattice simulation (i.e. with some redundancy) is shown to be less than for the nominally equivalent cascade of allpass sections.

It should be noted, in sections 4.1.1 and 4.4.2 that a better solution for the generation of allpass transfer functions has been found. The novel procedure is outlined in section 6.2.1 and demonstrated in practice in appendix A.

I have touched upon a number of theoretical issues for the novel CMWA topology. The novel Current Mode building blocks defining the CMWA topology have been described in some detail, both for the ideal case and in the presence of various errors in the building blocks. Several properties which are unique to CMWA filters have been described as well as some effects more generally valid for Wave Active filters.

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Chapter 5

Performance of filter implementations

This chapter gives detailed descriptions of a few transistor–level designs together with results. In one case the results are measured from integrated circuits, but in most cases the results are simulation results.

The first section describes the transistor–level designs of the elementary building blocks for first order integrator based filters in GaAs technology. The next section gives details of the first fabricated Continuous Time CMWA filter, a chip containing two fifth order lowpass Chebyshev filters simulated with first order integrators in CMOS technology. The last section gives first the details of building blocks for both first and second order based filters, and then describes a linear phase bandpass filter design in BiCMOS technology.

5.1 GaAs transistor level designs

As discussed in section 1.2.2, the initial project brief was to generate Giga–Hertz frequency filters in Gallium Arsenide (GaAs) technology. After the discovery of the CMWA filter topology, the GaAs work was stopped, but a series of designs was done, in order to assess the usefulness of the GaAs technology for CMWA filters. The specific technology originally considered is the GEC–Plessey F20 GaAs MESFET process which has FETs with gate lengths of $0.5\,\mu$m, gate widths above $18\,\mu$m and an f_T of approximately 20 GHz. The results were all reached using computer simulations. The transistor models used were partly the `SPICE` level 1 large–signal model and partly the AC model supplied by the manufacturer. The AC data were the results of careful characterisation — for common–source configuration — and thus fairly reliable for AC analysis of the complete designs. On the whole, the available transistor model data was not sufficient to make the simulation results very reliable.

Integrated GaAs MESFET circuits have found many applications in microwave designs where the speed of available GaAs technologies has been just ahead of silicon technologies for a long time. Typical applications are amplifiers for receivers/transmitters in frequency bands between 1 GHz and 15 GHz. GaAs MESFETs have very high output conductance (very low gain) at high frequencies, which means that the integration of traditional high quality OTA–C filter structures is very difficult. Examples of the complexities encountered are given in [5.9, 5.10, 5.11], where it is evident that the high complexity is *not* rewarded with superior performance. Except for considerations which are secondary to my project (e.g. radiation hardness), GaAs MESFET technology eems to have very little to offer for integrated filtering.

The CMWA topology does have the ability to cope with OTAs with low output impedance, thus reducing the complexity of the amplifiers drastically when using GaAs. On the other hand, the design of the current mirrors becomes a serious problem, since F20 MESFETs are only available as N–type depletion devices, making AC operation (and the combination of signal inversion and non–inversion) very difficult to achieve.

5.1.1 Linear tunable OTA

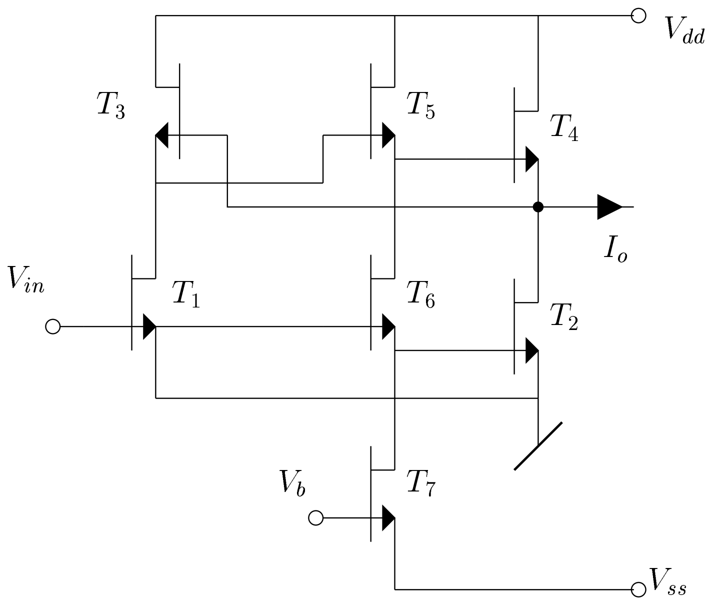

Figure 5.1: GaAs linear transconductor

The OTA selected is a simple tunable version of one linearised circuit given in [5.4]. The schematic is given in figure 5.1. The basic transconductor consists of transistors T_1 – T_4, with $T_{1/2}$ producing identical drain currents and $T_{3/4}$ working as a non–linear inverting mirror. The non–linearities of the voltage to current conversion of $T_{1/2}$ is countered by the non–linearity of the inverting mirror, producing a linear output current[1]. The transistors $T_{5/6}$ provide a fixed voltage drop across their gates, enabling the OTA to be tuned via the controlling input V_b. With V_D the maximum value of V_{GS}, the input voltage V_{in} may be in the range $[V_T - V_b; V_D]$ giving a useful range of $\pm V_D$ independently of the tuning, since $V_D < |V_T|$ by a substantial margin in most processes (e.g. $V_T = -2$ for GEC–Plessey F20, with $V_D \approx 0.5$). It should be noted that, because of the linearisation scheme, the output node is connected to a transistor gate; since the gate–source parasitic capacitance is dominant

[1]It should be noted that this linearisation technique assumes that the output conductance of the transistors is zero; in the case of GaAs MESFETs an assumption which is quite unrealistic. A general, and more mature, linearisation scheme is described in [5.3]

for these transistors (by more than a factor 10), the parasitic capacitance of the OTA as such is practically doubled.

About the performance, it suffices to note that the amplitude characteristic of the I_o/V_{in} response begins to deviate from a straight line just above 5 GHz. This corresponds to a substantial phase shift at 1 GHz, making operation in the microwave frequency bands very difficult.

5.1.2 Current duplicators

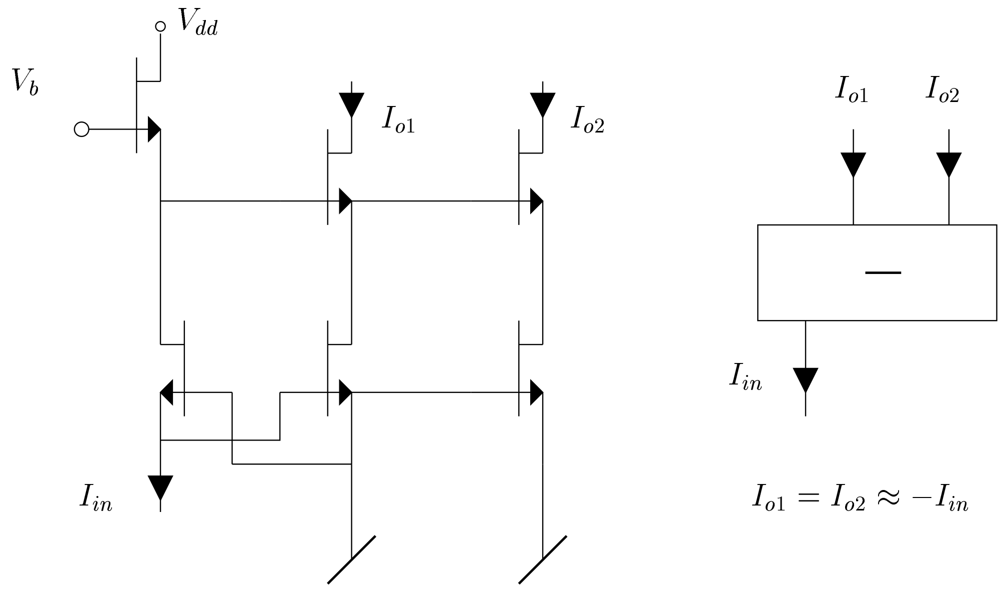

Figure 5.2: GaAs cascoded dual output current mirror, schematic and symbol

In Current Mode Wave Active filters, the quality of the current duplicators is quite important, so non–trivial design techniques have to be used. The main problems are the absence of P–type devices, the fact that depletion mode devices only are available and the high output conductance of the MESFET at high frequencies. In order to counter the problem of using only N–type depletion mode transistors, strange designs have to be used for the current mirrors. The cross–coupled pair [5.4], which implements an inverting non–linear negative current mirror, is used throughout. In order to decrease the output conductance, single cascoding is used.

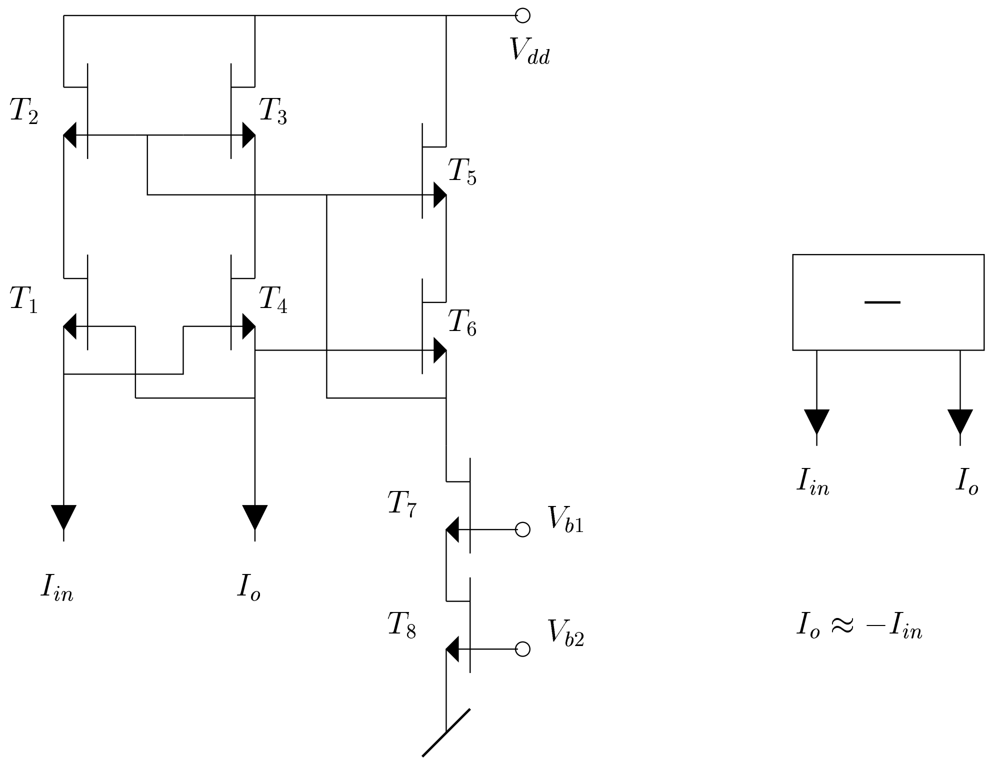

Figure 5.3: GaAs cascoded single output current mirror, schematic and symbol

In figures 5.2 and 5.3 I show the two current mirror building blocks. It should be noted that these blocks are non–linear on their own. Whether the combinations used in the complete duplicators are linear is considered irrelevant. The complete current duplicators are given as combinations of the primitive current mirrors in figure 5.4. While the dual output mirror is quite simple, the cascoding used in the single output current mirror is slightly complicated. This particular cascoding technique, the so–called self–bootstrapped cascoding, is described in [5.8].

The transistor sizes in the dual output current mirror can be set to any value (all six transistors identical). In the single output negative mirror, however, the cascoding requires the transistors to be sized with some care. The output transistor in the current mirror is T_4, with T_6 providing the biasing for the

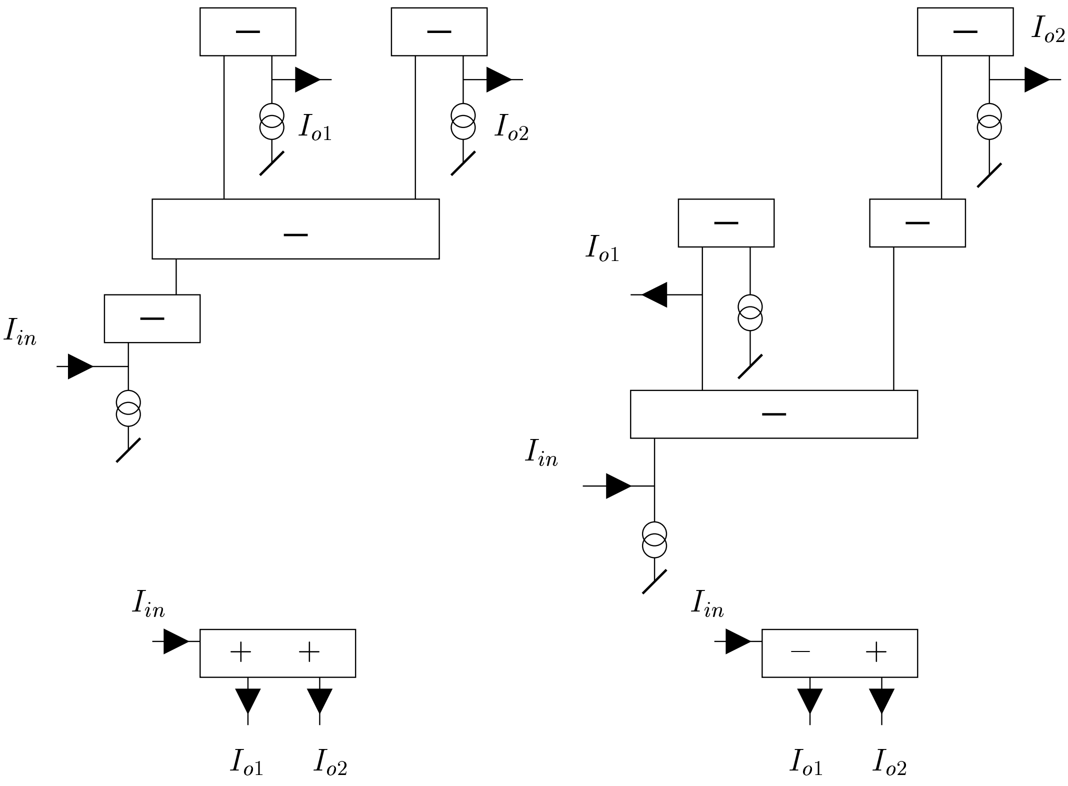

Figure 5.4: Schematics of GaAs versions of duplicators

cascode transistors T_2 and T_3 (T_5 bootstraps T_6 to improve the performance). Transistors 1, 4, 5, 6, 7 and 8 should be minimum size (for economy reasons), with transistors 2 and 3 having same gate length but larger gate width.

The drain–source voltage of T_4 is $-(V_{GS6} + V_{GS3})$. When the current flowing through T_5 and T_6 is sufficiently small, and T_3 has a sufficiently larger width than T_4, the drain–source voltage for T_4 is always larger than the limit for saturation, i.e. the cascoding works. To find the minimum necessary gate width for T_3, I assume $V_{GS3} = V_T$ and all gate lengths identical. Since the requirement for saturation is $V_{DS4} \geq (V_{GS4} - V_T)$, the gate–source voltage of T_3 must be smaller than $-V_{GS4}$. So, by setting the gate width of T_3 large enough to handle maximum current in T_4, I get the necessary minimum width. With the maximum current through T_4 determined by a maximum gate–source voltage of V_D, I get the maximum allowed gate–source voltage of T_3 to be $-V_D$. This sets the gate width of transistor T_3 as follows:

$$\begin{aligned} I_{Dmax} &= K\,W_4\,(V_D - V_T)^2 = K\,W_3\,(-V_D - V_T)^2 \\ \frac{W_3}{W_4} &= \left(\frac{V_D - V_T}{-V_D - V_T}\right)^2 = \left(1 - \frac{2V_D}{V_D + V_T}\right)^2 \end{aligned} \tag{5.1}$$

For the example technology, GEC–Plessey F20, the numbers are approximately $V_D = 0.5V$, $V_T = -2.0V$, giving $W_3/W_4 > 2.8$. In the simulations, a ratio of 3 was used.

Again, the performance is quite unexiting. The bare current mirrors have -3 dB frequencies in the range 3 – 8 GHz; the combination into duplicators would produce even slower circuits. The number of transistors in each duplicator is quite large, 27 transistors in the duplicator with two positive outputs and 30 transistors in the duplicator with both polarities. The area consumption is approximately 0.25 mm by 0.25 mm for either duplicator (assuming the use of transistors with 18 μm gate width).

5.2 Fabricated CMOS chip

To provide a simple proof of concept, a CMOS technology circuit was designed and submitted for fabrication. The measured results form the experimental verification of the CMWA filter topology and confirm the main points of the theory[2]. The filter specification in itself was not meant to be spectacular, but frequency range was prioritised during the design (to provide measured data relevant to the effects of high frequency errors discussed in chapter 4). The passive prototype is a fifth order polynomial lowpass filter with Chebyshev passband characteristic. On the chip there are two filters, identical except for the cutoff frequencies which are 3 MHz and 30 MHz.

[2]Since the implementation is based on first order integrators, only this part of the theory is confirmed — of course

The technology is the ORBIT $1.2\,\mu$m double–poly double–metal CMOS process. In order to use a technology with such a small feature size, the supply voltage is kept to ± 2.5 V; the choice of a technology with small feature size is dictated by a desire to design circuits which are relevant for mixed–mode designs. The design was performed using the supplied data for the `SPICE` level 2 model. Thus, the results are not completely reliable (particularly for transistors with short gates — less than $2\,\mu$m — in the computation of the G_{DS} impedance of the MOSFETs).

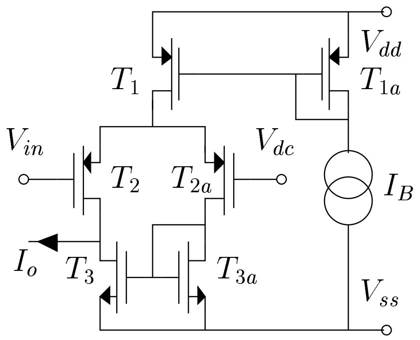

Figure 5.5: CMOS OTA

5.2.1 Basic building blocks

The amplifier is a simple long–tailed pair input stage with the two output currents combined into one with a current mirror. The second input can be used to control DC offset. The OTA is shown in figure 5.5. The linearity of this design is not very good, but the frequency performance is good. The design transistor widths are given in table 5.1. All bulk nodes are connected to their corresponding supply rail.

Transistor	width @3 MHz	width @30 MHz
T_1	54	81
T_2	16.2	54
T_3	18	36

Table 5.1: Transistor widths in CMOS OTA. All transistor lengths 1.8. All units μm

At 3 MHz the nominal bias current is $I_B = 120\,\mu$A giving a transconductance of $G_m = 123\,\mu$A/V; for 30 MHz $I_B = 300\,\mu$A, $G_m = 410\,\mu$A/V. The large signal behaviour is optimised for the low frequency filter, with the output able to drive ±1 V and the bias current sufficient to allow the same input range. The size of an amplifier for the 3 MHz filter in the layout is 82 by 50 μm.

The current duplicators use single cascode current mirrors, with the signal flowing through N–type transistors only (thus improving frequency performance at the cost of one more chain of transistors). The schematic for a duplicator with both inverting and non–inverting outputs is shown in figure 5.6. (For a duplicator with two non–inverting output, the only difference is a different internal connection of the signals.)

For the design the transistor widths were $30\,\mu$m for the N–types and $75\,\mu$ for the P–types, with the lengths being $1.2\,\mu$m in both cases; this gives an output voltage range of the desired ±1V. Performing a very simple analysis, the upper frequency limit factor G_m/C_{GS} is found to be proportional to $(V_{GS} - V_T)$ and inversely proportional to L^2 (with L the gate length)[3]. So, the sizing is a simple matter of chosing minimum gate length and setting V_{GS} as high as possible (for the operating point). The upper limit for V_{GS} is set by the required output

[3]Assuming that the frequency limit is set by the input RC time constant C_{GS}/G_m, that C_{GS} is proportional to the gate area and that G_m can be computed from the simple expression $I_{DS} = K(V_{GS} - V_T)^2 W/L$ with K a constant

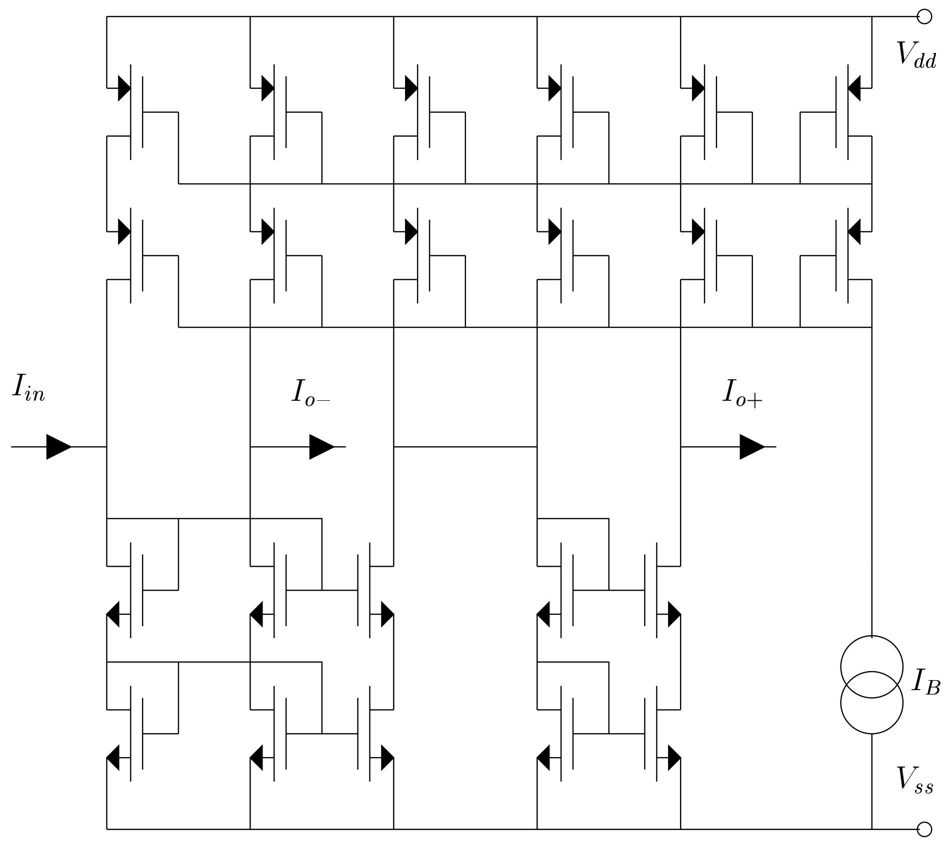

Figure 5.6: CMOS current duplicator, inverting output I_{o-} and non–inverting output I_{o+}

voltage range, which concludes the sizing considerations. For the operating point, the input impedance is $3.6\,\mathrm{k\Omega}$, the output impedance $1.2\,\mathrm{M\Omega}$, the transfer ratio $\lambda = 0.995$, the -3 dB frequency 180 MHz for the non–inverting output and 400 MHz for the inverting output. The size of either type of duplicator in the layout is a width of 0.22 mm and a height of 0.11 mm.

Each two–pair is 0.46 mm wide and 0.24 mm tall; this includes space for an integration capacitance of about 3.4 pF (a larger capacitance simply makes the complete structure wider, as seen in the chip photo 5.10). The two–pairs are tuned by biasing currents which are duplicated to all identically connected amplifiers, i.e. all selfconductance connected OTAs are controlled by I_{B1} and all transconductance connected amplifiers controlled by I_{B2} generating G_{m1} and G_{m2} respectively. (The generators marked I_B in figure 5.5 are outputs of uncascoded current mirrors, i.e. the actual I_B values are probably not identical to the currents input to the chip.)

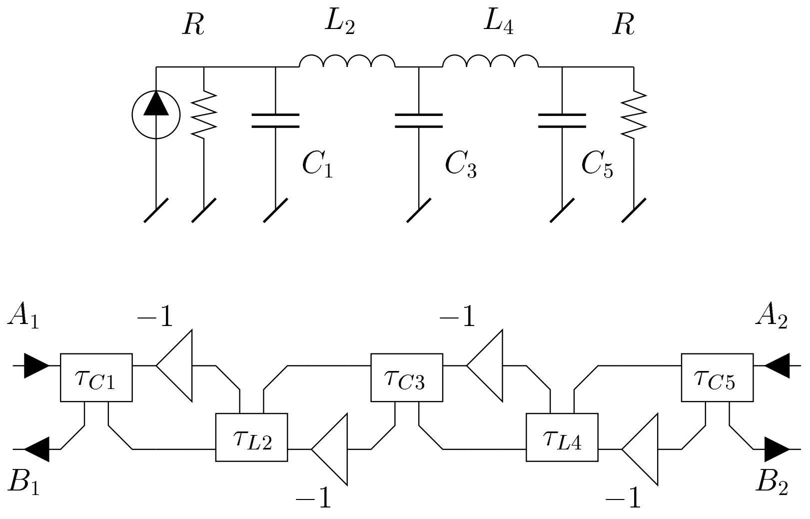

Figure 5.7: Fith order lowpass filter, prototype and CMWA simulation

Component	Prototype value	τ	C value @ 3 MHz	C value @ 30 MHz
C_1, C_5	2.32	1.16	7.56 pF	2.43 pF
L_2, L_4	1.035	0.5158	3.37 pF	1.00 pF
C_3	3.205	1.602	10.46 pF	3.12 pF

Table 5.2: Normalised prototype component values and time constants for $R = 1$; integration capacitance values with $G_m = 123\,\mu$A/V @ 3 MHz and $G_m = 363\,\mu$A/V @ 30 MHz

5.2.2 System design

The prototype is a simple polynomial lowpass filter with component values set for Chebyshev passband characteristic with 1.25 dB passband ripple. The prototype, together with the Wave Active simulation is shown in figure 5.7; the component values, from [5.6] design T0550, are given in table 5.2.

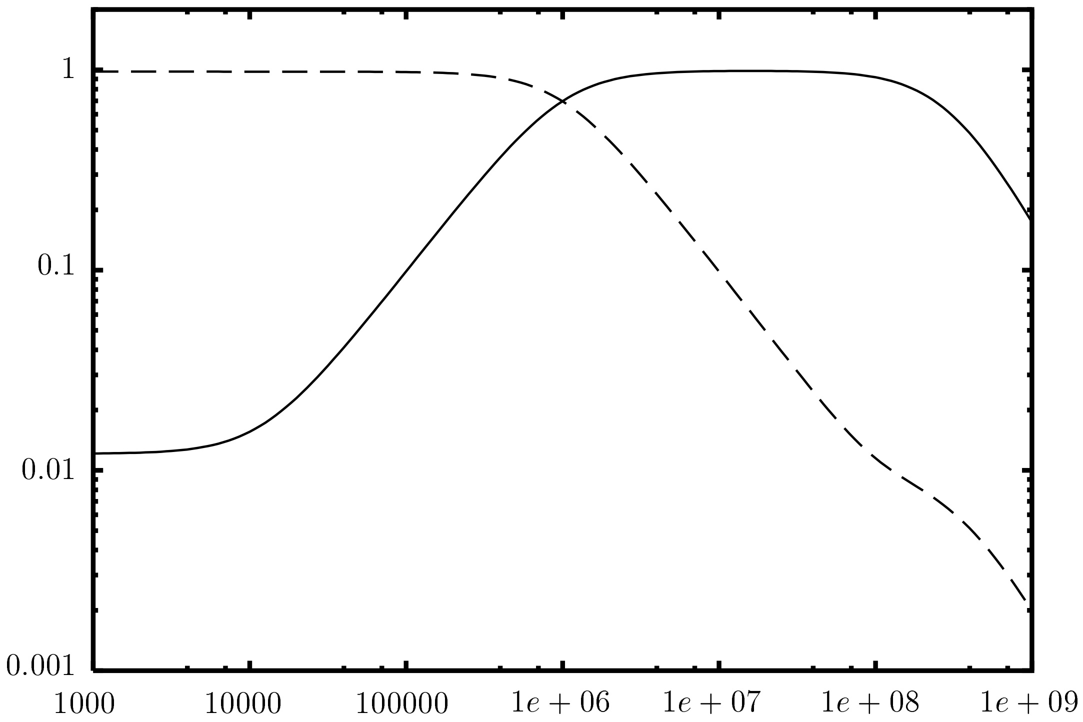

Figure 5.8: Simulated transfer functions of two–pair tuned to 1 MHz, B_1/A_1 (solid) and B_2/A_1 (dashed). X axis frequency in Hz, Y axis amplitude

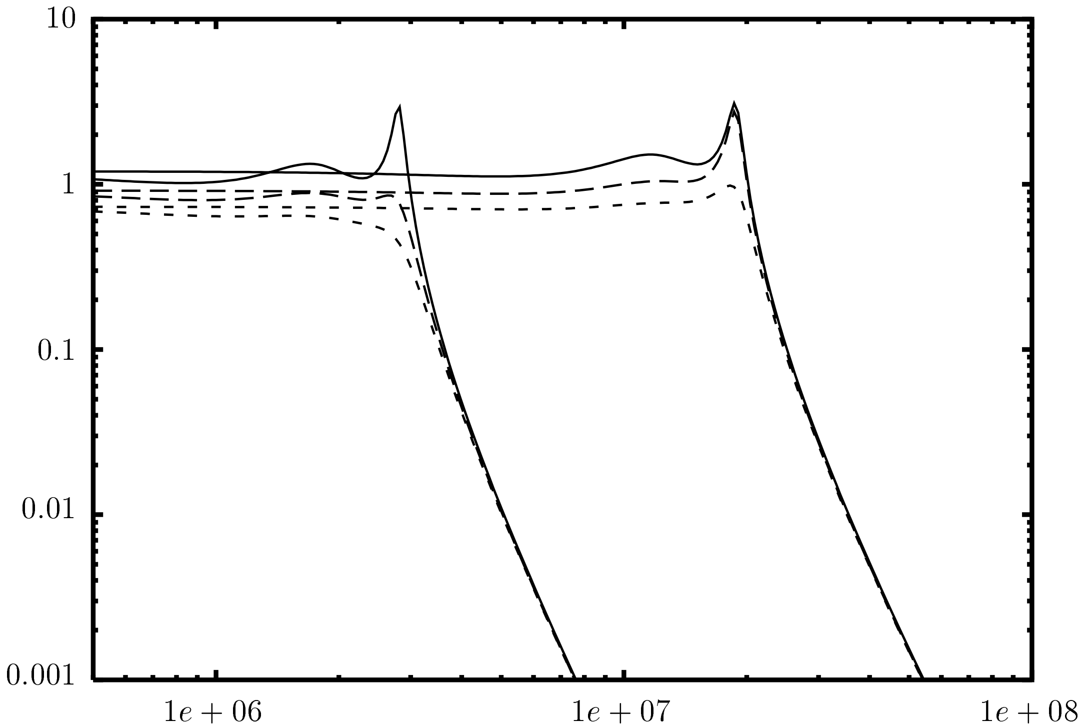

Figure 5.9: Simulated lowpass transfer functions for 3 MHz and 30 MHz filters, showing phase tuning; $I_{B1} = 80.5\,\mu$A, $90.5\,\mu$A, $100.5\,\mu$A for top, middle and bottom curves. X axis frequency in Hz, Y axis amplitude

Chip microphotograph goes here

Figure 5.10: Microphotograph of CMOS chip

The nominal tuning was decided by simulating a single two–pair and minimising B_1/A_1 at low frequencies. The resulting frequency response (for a two–pair set to have a cutoff at 1 MHz) is shown in figure 5.8. Setting the biasing of the complete filter to the values found in this way is equivalent to tuning the amplifiers without taking into account the effects of HF errors. The cutoff frequency of 3 MHz was found as the highest value where the peaking of the response, in simulation, was smaller than the nominal passband ripple (effectively doubling the passband ripple). In figure 5.9, we show the lowpass responses for the 3 MHz design as well as for a fictive 30 MHz design[4], with I_{B1} set to $80.5\,\mu$A, $90.5\,\mu$A and $100.5\,\mu$A (for $I_{B2} = 120\,\mu$A), the middle value be-

[4] Not the actual design where the amplifiers are larger, but the same design with the integration capacitors set a factor 10 smaller

ing the nominal design value. The filter with a cutoff frequency of 30 MHz has a peaking of approximately 10 dB when tuned in this way, indicating that tuning has to be performed to counter the effects of HF errors for high frequency designs (which is what we expect from the results in section 4.3.3).

Dual Xfer function pic goes here

Figure 5.11: Measured responses, lowpass B_2/A_1 and highpass B_1/A_1

The complete chip is shown in figure 5.10. The chip area is slightly less than $1.8\text{mm} \times 1.8\text{mm}$ with the two filters taking up equal amount of space. One two–pair, tuned to the cutoff frequency of the corresponding filter, are added for each filter. The 3 MHz filter takes up the top half of the chip. Half of the external connections are power supply lines, all V_{DD}, V_{SS} and ground lines carried on unbroken lines of metal. For each of the four CMWA filters, the A_1 and $B_{1/2}$ lines are connected to the pins.

Only the 3 MHz filter was measured (because of limitations in the measure-

F tuning pic goes here

Figure 5.12: Measured response, three different cutoff frequencies

ment setup, see appendix E). The two main transfer functions, as shown in figure 5.11, confirm that the filter works. The bias currents controlling I_{B1} and I_{B2} were $104\,\mu$A and $124\,\mu$A respectively. It is clear — from the difference in flat levels for the lowpass and highpass transfer functions of 5 dB — that the effects of HF errors in the building blocks is more severe than anticipated. It should be noted that it is possible to tune the chip to get deeper notches in the highpass transfer functions.

The ability to tune cutoff frequency is verified by the measurements in figure 5.12. The bias current pairs were $78\,\mu$A $89\,\mu$A, $104\,\mu$A $124\,\mu$A and $257\,\mu$A $550\,\mu$A for the frequencies 2.7 MHz, 3 MHz and 3.7 MHz respectively. It should be noted that all tuning points were chosen for 1 dB passband ripple, at the same level as the nominal curve from figure 5.11. The middle peak on the

Q tuning pic goes here

Figure 5.13: Measured response, three different Q tuning points

response is more pronounced for the lower cutoff frequencies, indicating that the deterioation of the shape is a result of the phase tuning — i.e. that the restoration of transfer function shape is not perfect.

The phase tuning process changes the level at the passband edge, as indicating in figure 5.13. These traces are for the fixed value of $I_{B2} = 124\,\mu$A with I_{B1} having the values $122\,\mu$A, $104\,\mu$A and $97\,\mu$A for the attenuated, nominal and peaky responses respectively.

The main conclusion from the measured results is that the need for Q tuning exceeds the expectations. The two graphs in figure 5.9 indicate that a factor 10 in cutoff frequency can lead to a large difference in peaking level (in this case 10 dB). The flat level for the most attenuated graph for the 30 MHz design in figure 5.9 is 3 dB down from the nominal value; this indicates that the 5 dB difference observed in figure 5.11 is equivalent to the simulated response for a filter with a cutoff frequency in the range $10 - 30$ MHz (very roughly). The bias current used also bears this out, with the flat response observed for the bias current pair $104\,\mu$A $124\,\mu$A (which is approximately the necessary levels to get flat response for the 30 MHz filter in simulation, indicated by figure 5.9). Thus, we conclude that the simulation is optimistic, by a factor of roughly 10 for the high frequency limitation of the building blocks. This is not entirely unexpected since we only had level 2 model data for the design.

5.3 BiCMOS transistor level designs

In the previous sections designs based purely on FET transistors have been described. The bipolar transistor — with its intrinsic higher gain — is better suited to the design of current mirrors, whereas FETs are perfectly suited for the design of OTAs. The combination of bipolar and FET transistors therefore seems to offer the ideal combination for CMWA filters. Through the kindness of BNR/nt[5], the model parameters for the BATMOS5 process — a $0.8\,\mu$m BiCMOS process with $f_T = 14$ MHz — were made available and several designs were done. (One chip, with single amplifiers and current mirrors, was actually fabricated; time constraints unfortunately prevented the necessary measurements.)

The model parameters for the MOSFET transistors were for level 3 models (with different sets of model data for different ranges of gate lengths) and therefore not the most reliable for analogue simulation[6].

[5]Bell Northern Research / northern telecom. The research and main branches, respectively, of the Canadian telecommunications company

[6]The use of the two different models for a gate length at the border between two intervals produced very different values for output conductance in the operating point

5.3.1 Basic Building Blocks

With both MOSFETs and bipolar transistors available, the two types are used for the purposes that fit their abilities. Thus, the MOSFET transistors are used for the input transistors in the OTAs and bipolar transistors are the active elements in the current mirrors. Since only vertical NPN bipolar transistors were avilable, all bias current supplies are regulated cascode [5.5, 5.7] current mirrors with P–type MOSFETs.

The OTA for use in first order based systems is a BiCMOS OTA using one N–type MOSFET in triode region operation in the input and an N–type bipolar transistor stabilising the drain voltage (thus both securing triode region operation *and* providing cascoding to increase output impedance). The OTA is described in detail in [5.2]. The schematic is shown in figure 5.14; $Q1$ is a single NPN transistor and the sizes of the MOSFETs are shown in table 5.3. The nominal bias current is 0.5mA and the nominal bias voltage $V_{B1} = -0.5$V giving a transconductance of 0.4mA/V over an input range of approximately ± 0.5V with acceptable linearity for a supply voltage of ± 2.5V. The high frequency rolloff occurs at 2 GHz, the output impedance is 4 MΩ, the input parasitic capacitance is 0.04 pF and the output capacitance is 0.4 pF.

Transistor	width	length
$M1$	10	2
$MB1, MB2, MB5$	200	2
$MB3$	24	1.2
$MB4$	12	1.2
$MB6$	100	2

Table 5.3: Transistor sizes in BiCMOS OTA. All units μm

The OTA for use in second order based systems is a dual–input dual–output structure derived from a pure bipolar OTA described in [5.12] (the only change is to use a MOSFET input transistor to increase the input impedance). The schematic is shown in figure 5.15. The input stage consists of the N–type

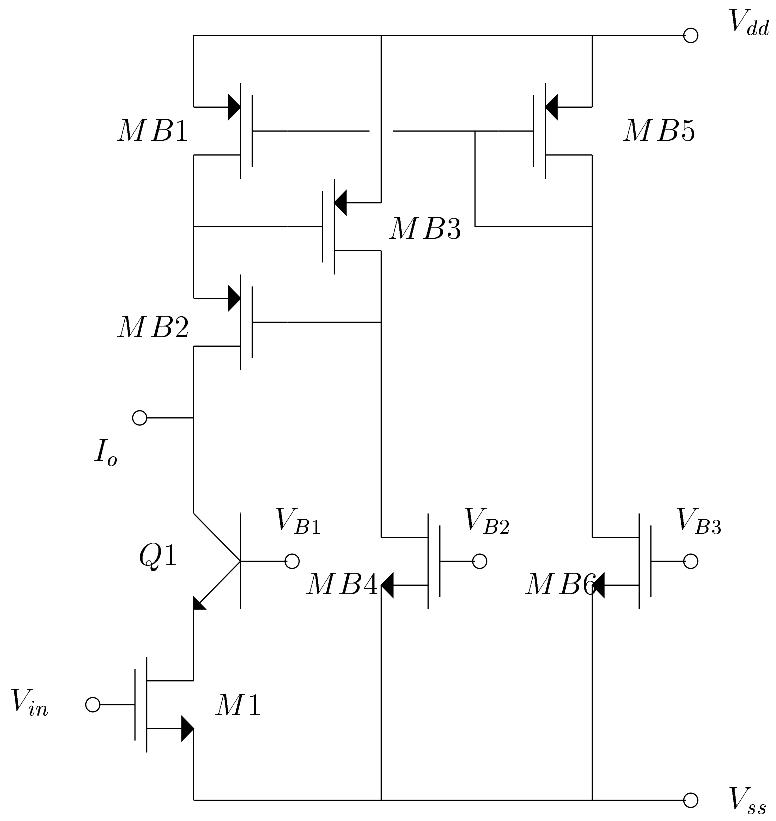

Figure 5.14: BiCMOS one–input one–output OTA

MOSFET $M1$ and the degeneration resistor Rd. The bipolar transistors $Q1$ – $Q2$ transfer the signal current to the output. The input voltage range is ± 0.5V with very good linearity. The transconductance is tuned by setting the two tail–currents (in $Q1$ and $Q2$ respectively) differently (in the original design, the nominal values were identical currents for the two transistors; setting the bias currents differently in the nominal operating point compensates for the fact that the input is a MOSFET rather than bipolar transistor). The supply voltages are -3V and 2V. The input voltages do not have to be symmetrical to ensure linear operation. The top bias supplies to the output are identical to those in figure 5.14; the bottom bias supplies are compensated bipolar mirrors with the ability to operate at very low voltages (down to 0.3V off the supply rail). The output is cascoded to ensure high DC gain. For the nominal bias point — where the bias current for the input stage is 0.7mA and 0.8mA for the output stage — the transconductance is 0.6mA/V ($I_{o+}/(V_{i+} - V_{i-})$). The input parasitic capacitance is 0.6 pF, the output parasitic capacitance is 1.1 pF and the output impedance is 10 MΩ; the HF rolloff occurs at 1 GHz.

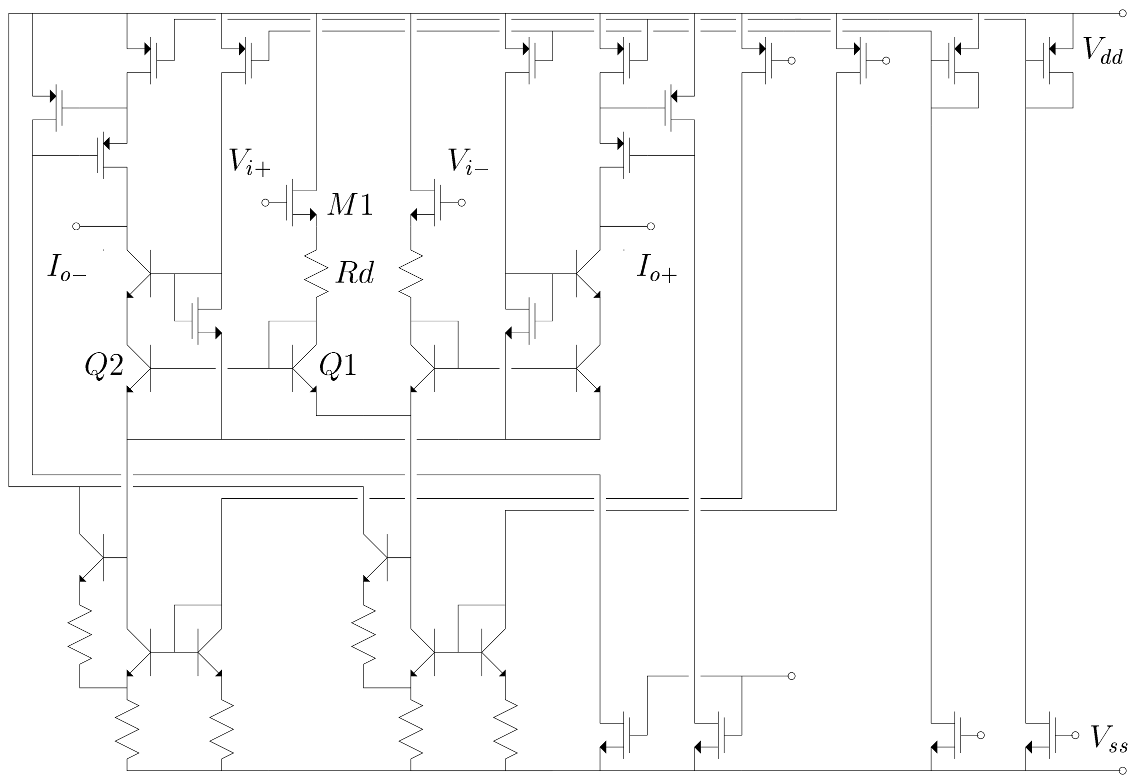

Figure 5.15: BiCMOS dual–input dual–output OTA

The current duplicator uses bipolar transistors exclusively in the signal path (and the usual MOSFET bias current mirrors). The schematic is shown in figure 5.16; the current mirrors use seperate transistors for β compensation. The resistive degeneration increases the output impedance and has a nominal degeneration voltage of 0.026V (0.26mA into 100 Ω); all the bipolar transistors are single N–type transistors. The input impedance is 0.34 kΩ , the output impedance is 420 kΩ and the output parasitic capacitance is 0.3 pF. The transfer ratio is 1.001 and the HF rolloff occurs at 1.5 GHz (for the inverting output).

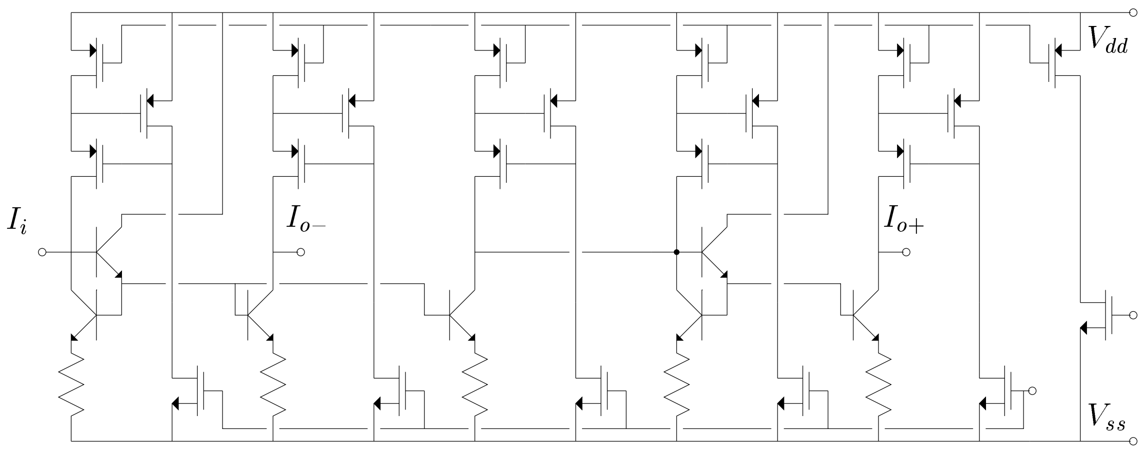

Figure 5.16: BiCMOS current duplicator

5.3.2 Linear Phase bandpass filter

The filter designed from the characteristics of the BiCMOS building blocks is a linear phase 12th order bandpass filter. The normalised specification is flat amplitude response in the range 0.8 – 1 rad/s. The group delay is to lie within a range of 2 s in the frequency range 0.773 – 1.033 rad/s. The stopband behaviour is that of a fourth order polynomial bandpass filter with -20 dB points at 0.53 and 1.5 rad/s. The prototype design was performed by using a numerical optimiser in the package APLAC [5.1]; as a consequence of using a direct optimiser (rather than designing a frequency response is the s domain), the responses are not perfectly equi–ripple. The prototype filter is shown in figure 5.17 with the component values shown in table 5.4. The passband amplitude and group delay responses are shown in figure 5.18.

The integration capacitor values for the actual filter was found by using the building block data found above and designing for increasing centre frequency. (The numerical optimiser was unable to compensate for the errors in just one run; so, by increasing the centre frequency in steps, we introduce the effects of high frequency rolloff gradually and enable the optimiser to converge.) The nominal and final capacitance values are shown in table 5.5 with C_{11} being

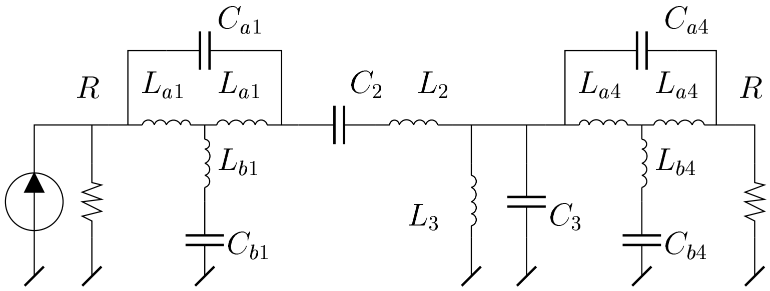

Figure 5.17: Prototype linear phase bandpass filter

Prototype component	value	Prototype component	value
C_{a1}	2.16	C_2	5.46
C_{b1}	1.03	L_2	0.240
L_{a1}	0.297	C_{a2}	1.38
L_{b1}	1.13	C_{b2}	0.625
C_1	0.322	L_{a2}	0.366
L_1	3.80	L_{b2}	1.57

Table 5.4: Normalised component values for prototype linear phase bandpass filter ($F_0 = 1$ rad/sec, $R = 1$)

capacitor C_1 in the S' allpass section simulating the first block, C_{32} being C_2 in the bandpass biquad simulating C_2 L_2 and so forth. The passband response of the final filter, set to an upper cutoff frequency of 5 MHz, is shown in figure 5.19 with the stopband performance shown in figure 5.20. The effect of HF rolloff is a steeper rolloff in the upper stopband.

To get an impression of the sensitivity of the design, we performed a Monte Carlo analysis and recorded the simulated yield. We assume a deviation of $\pm 0.75\%$ (flat distribution) for the primary values (C, A and G_m) and a deviation of $\pm 15\%$ for the parasitics (parasitic capacitances, output impedances and HF rolloff frequencies). The acceptance region is set to group delay within the range [$0.96\,\mu$s, $1.06\,\mu$s] in the frequency range [3.87 MHz, 5.17 MHz]; the amplitude smaller than -18 dB below 2.65 MHz and above 7.5 Mhz and within the range [-0.75 dB, 0.25 dB] in the frequency range [4 MHz, 5 MHz]. With

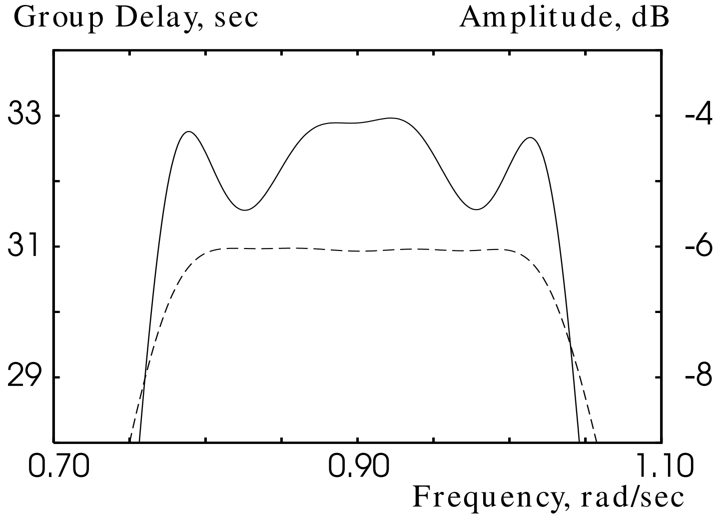

Figure 5.18: Response of prototype linear phase bandpass filter. Upper trace groupdelay, lower trace amplitude

400 Monte Carlo sweeps, the simulated yield was 49%; this indicates that the design is not excessively sensitive. A more sophisticated model of manufacturing imperfections would allow for a proper yield optimisation. (It should be noted that if the building block imperfections are not taken into account — i.e. if the original capacitance values are used — then the performance is dramatically worse, the group delay ripple is more than 10 times larger than the range above!)

Cap	original	compensated	Cap	original	compensated
C_{11}	3.3 pF	4.7 pF	C_{41}	30.4 pF	19.7 pF
C_{12}	48.1 pF	36.7 pF	C_{42}	5.4 pF	7.4 pF
C_{21}	5.7 pF	6.7 pF	C_{51}	4.1 pF	4.0 pF
C_{22}	28.5 pF	26.5 pF	C_{52}	30.8 pF	29.4 pF
C_{31}	21.2 pF	27.6 pF	C_{61}	3.4 pF	3.3 pF
C_{32}	7.2 pF	5.3 pF	C_{62}	39.1 pF	36.4 pF

Table 5.5: Capacitance values in CMWA bandpass filter. $F_0 = 5$ MHz, $G_m = 350\mu$A/V

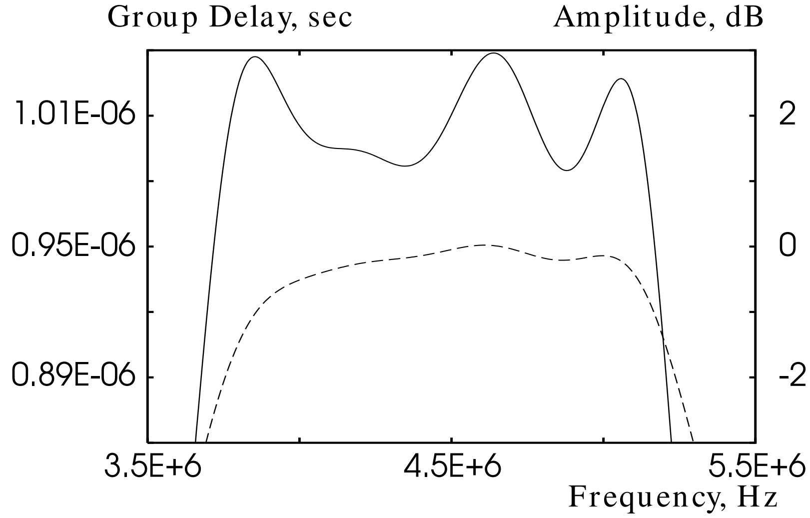

Figure 5.19: Passband performance of final CMWA bandpass filter. Upper trace group delay, lower trace amplitude

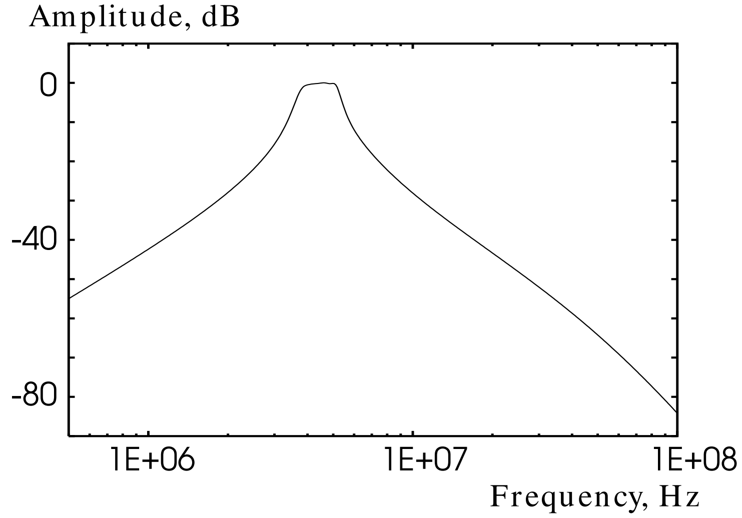

Figure 5.20: Stopband amplitude response of final CMWA bandpass filter

5.4 Discussion and conclusion

The GaAs MESFET technology circuits proved to be a disappointment. Since commercial fabrication of GaAs is very much more expensive than for silicon technologies, the results, *in this application*, do not justify the use of GaAs.

The CMOS chip demonstrates that the basic properties predicted by simulations hold in actual measurements. While the filters on the chip are not claimed to be the best Continuous–Time integrated filters ever, the fact that the filters work at all are a strong indication of underlying soundness.

The BiCMOS design demonstrates that very good performance is available in the cases where the process offers features suited to both types of active elements. In particular, filters based on first order integrators would be compact and have very good performance. The complete design demonstrates high performance for a modest frequency, one possible way of exploiting the features of the process (an other way is to build filter of average performance for very high frequencies). As ever, for the Lattice simulation blocks, section 6.2.1 should be taken into account. In other words, the filter described in section 5.3.2 is somewhat obsolete.

Although the experimental results are not the core of the results of this work, as a whole they indicate high potential. The actual measured results confirm the simulation results, which is what was required. The simulated results indicate a good performance potential.

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Chapter 6

Discussion and conclusion

This thesis does not claim to be an exhaustive study of the CMWA topology. The main resons for the lack of completeness is the simple fact that only a limited amount of time was available for the work. For a project with insufficient time, some choices about the actual contents have to be made. In the case of this thesis, I have chosen to look into a number of different topologies (using simulation rather than building filters). For this reason, the achieved practical results do not demonstrate the best performance for any integrated filter ever. Also, the theory has suffered from lack of work, with many interesting aspects being ignored because of lack of time. On the other hand, a lot of new material has been presented, serving perhaps as a starting point for good work in the future.

6.1 Achieved results compared to state of the art

The achieved results fall in two categories — the theoretical and measured results for the first order based filters and the theoretical results for filters based on biquads.

The filters based on first order two–pairs demonstrate, theoretically and in practice, a number of properties different to those of conventional OTA–C filters

- The ability to compensate for OTA phase and gain errors by simple tuning of OTA transconductance gain
- Through the use of two different active building blocks, the design procedure has a different set of priorities, i.e. the variable gain elements (OTAs) do not need high DC gain and the elements which do need high output impedance (current mirrors) do not need to be tunable
- At the expense of a relatively large number of active devices, all prototypes are simulated with lossy first order integrators and without floating capacitors. The circuits have no nodes with high impedance — at DC or high frequencies — and all nodes either have a capacitor to ground or are (ideally) at virtual ground

The filters based on higher order two–pairs — in practice two–pairs with one or two biquads — demonstrate an alternative to "multiloop feedback" structures with the added ability to simulate Lattice sections with fairly simple circuits. Compared to cascade connection of biquads, CMWA filter benefit from having lower sensitivity, and — certainly in the case of bandpass filters — lower Q values.

6.2 Further Work

Prototype sections are still an interesting subject. The logical next step is a Brune type section built from first order lossy integrators — this would allow for the simulation of lowpass filters with finite transmission zeros without using prototype structures with redundant components. Other prototype structures, such as that shown very briefly in [6.4], could achieve the same goal. Another way of adding transmission zeros is to simulate the effect of the redundant capacitor by the use of amplifier circuits. While this is fairly simple for impedance simulations, it is difficult for Wave Active structures — but not impossible, as demonstrated in [6.1].

Practical issues are, however, the most pressing concern. The design of biquads using lossy integrators — perhaps mirroring the structure shown in figure **??** (from [6.5]) — should be considered for use in lowpass filters. Also very important is tuning circuits without which hardly any practical integrated continuous–time filter can be built. One existing tuning scheme which can be used directly is the use of two tuning quantities to tune centre frequency and maximum gain for a bandpass biquad (verbatim in a biquad based filter or based on two first order two–pairs in a first order based filter) in a master–slave arrangement. Higher precision can be obtained by tuning all biquad sections individually, in which case it is possible to benefit from the fact that the Q values are quite low and thus measurable — making schemes such at the T_{23} scheme from [6.8] possible.

For a filter topology based exclusively on Current Mode signal processing, the Log–domain filters of Frey [6.3] should be investigated as a way of building high precision filters in pure bipolar technology (which might very well work with low supply voltages). Wave filters based on Log–domain biquads with current Wave signals could provide the answer to synthesis of high order filters (rather than simple cascades as proposed so far) in pure Current Mode.

6.2.1 Implementing allpass blocks using two–pairs

One of the weaknesses of the Lattice simulation, as presented in [6.7, 6.6], is that conventional allpass filters are used as subblocks. Fortunately, it is possible to use the equivalent of a reactively loaded circulator to produce allpass

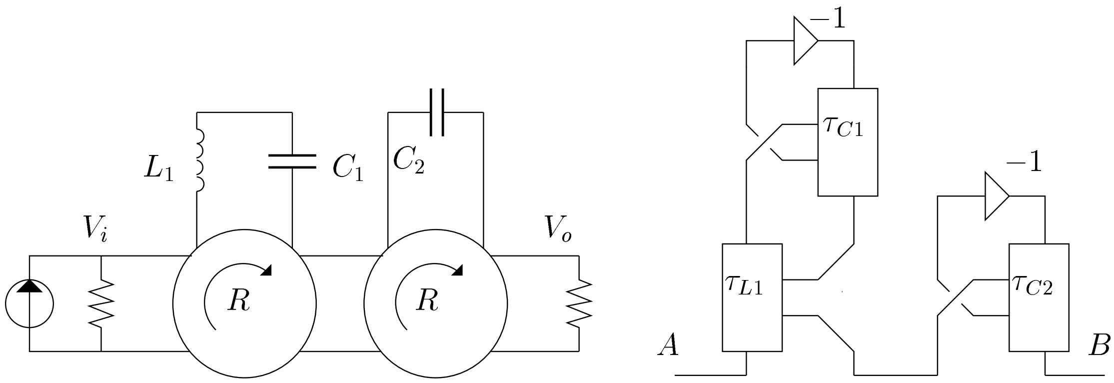

Figure 6.1: 3rd order unidirectional allpass filter and Wave Active equivalent. $B/A = 2\,V_o/V_i$

filters from Wave Active building blocks (two–pairs). I owe the realisation of this to a monograph by Dr Wupper [6.9], illustrations 4.32 and 4.33 (although the circuits are also given, for digital filters, in [6.2, section V.C]). The equivalentce is illustrated by figure 6.1, which shows a unidirectional allpass filter and the Wave Active equivalent. As shown in appendix A this equivalent is very useful for implementing linear phase filters having Lattice sections using only lossy first order integrators (or low–Q biquads, as the case may be).

6.3 Conclusion

This thesis has introduced the Current Mode Wave Active filter topology. Filters based on first order lossy integrators and filters based on biquads with low quality factors have been presented. This thesis should be seen as the start of the work on CMWA filters — rather than the final, complete, statement on this topology.

To sum up my own opinion of the work done; the worst aspect is that I should have spend more time on experimental work (the measurements on the CMOS chip were delayed for no good reason, making the presentation ill timed and the followup too late); the best aspect is the mix of exploratory work and fairly serious mathematical analysis, meaning that the scope of the complete project is quite wide without losing quality entirely.

A novel filter topology has been presented and the initial measured results confirm the theoretically predicted properties. Through the ability to simulate prototype topologies hitherto unrealisable in integrated filters, CMWA filter promise new levels of performance for linear phase integrated filters.

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Appendix A

A Linear Phase lowpass filter

As an example of the increased performance possible from prototypes using Lattice sections, we show a linear phase lowpass filter design based on an Hourglass approximation example filter [A.1]. *Note that the text in this appendix is taken directly from a paper written after the main text of the thesis was finished. As such, it includes material which makes parts of the thesis obsolete...*

A.1 Allpass filters built from first order lossy integrators

While we have, in earlier publications, indicated that the allpass sections needed for the simulation of Lattice prototype sections [A.4, A.3] can be built directly as OTA–C sections containing lossless integrators, a solution based on the same integrator sections as those used in the simulation of conventional filter sections is desirable. Recently, we have had access to a monograph [A.7] by Dr Wupper — one of the persons responsible for the first Active–RC Wave filters [A.5, A.6] — which contains some very interesting circuits for allpass filters. If a three–port circulator (a component which rotates the signals at the ports) is loaded at two ports with resistances and with an LC impedance at the last port, the transfer function between the two resistors (load and source impedance) is allpass. The LC impedance may be simulated using two–pairs, by observing that an impedance can be implemented as a ladder filter terminated by a short circuit, and may thus be simulated using two–pairs. A circulator–LC circuit defining a third order allpass filter is shown in figure A.1 together with the Wave Active simulation[1], as given in figures 4.32 and 4.33 in [A.7].

A.2 Linear Phase lowpass filter

As an example of the use of the second order allpass section, we show the linear phase filter from [A.1], given as an application of the Wave Active Lattice section simulation in [A.3]. The prototype is shown in figure A.2, using a second order Lattice section rather than the original network using two capacitors and two coupled coils. The filter has a 9th order transfer function with four zeros placed symmetrically around both axes in the complex plane, at a frequency within the passband; thus the amplitude response in the stopband is like that of a 5th order lowpass filter while the passband has equi–ripple approximation to constant groupdelay and an amplitude response with two maxima (one at DC and one in the passband). As shown in [A.2], designs with transfer functions of this type (non minimum–phase without allpass factors) achieve better performance — as measured in groupdelay and amplitude linearity — than conventional combinations of amplitude filters followed by allpass sections.

The Wave Active simulation is shown in figure A.3. The two–pairs labelled τ_{CA} – τ_{LB} form the allpass circuit simulating the second order Lattice section. The amplifiers marked 1/2 are implemented by having two transistors in parallel

[1] An inverter connected from B_2 to A_2 simulates the short circuit termination

in the input of the following current duplicator. The design is simulated with a cutoff frequency of 100 kHz, using the circuits from the CMOS filter, the OTAs having a transconductance of 129 μA (in a real design, smaller transconductance would probably need to be used to decrease the total capacitance). At this frequency, the filter works fine without any phase tuning, i.e. the biasing of the two OTAs in the two–pairs is deteremined by the DC transfer functions for the elementary two–pairs, which are $B_1/A_1 = 0.4\text{e-}03$ and $B_2/A_1 = 0.995$ for $I_{B1} = 93$ μA and $I_{B2} = 120$ μA. The simulations are performed with the accurate `BSIM` model parameters, using AC analysis. The prototype component values, time constants and denormalised capacitance values are given in table A.2 (please note that the time constant τ_{CA} is determined by the component L_2, and τ_{LA} by C_2; this is a consequence of the way the allpass equations are found).

For an ideal filter, the passband response specification is groupdelay in the range [12.731 μs, 12.813 μs] in the frequency range [0, 120 kHz] and amplitude in the range [-1 dB, 0 dB] in the frequency range [0, 100 kHz]. The result of a transistorlevel simulation is group delay in the range [11.914 μs, 12.174 μs] and amplitude in the range [-2.70 dB, -1.08 dB] for the same frequency ranges. Thus, the groupdelay ripple is almost four times larger and the amplitude ripple almost twice as large as the prototype. The frequency responses of both ideal and transistorlevel simulations are shown in figure A.4. While the achieved performance is not quite as good as the prototype performance, the results are still quite impressive. With more agressive optimisation, using building block characteristics or maybe full transistorlevel simulation, better performance should be reachable.

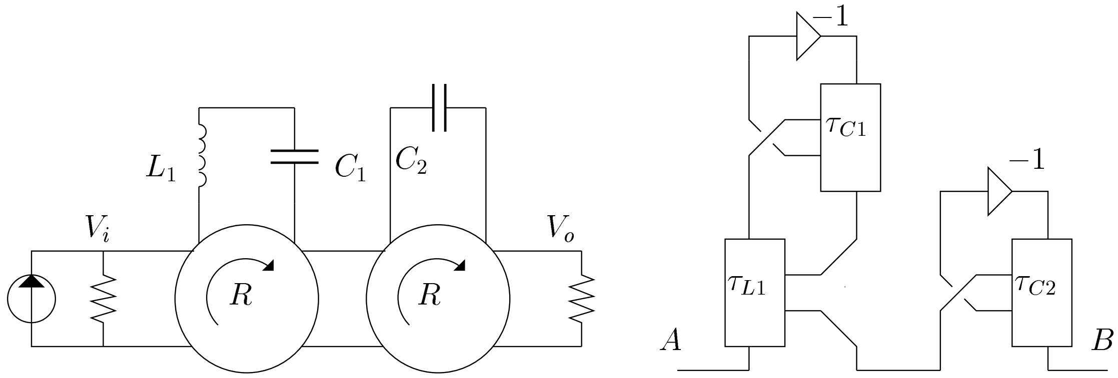

Figure A.1: 3rd order unidirectional allpass filter and Wave Active equivalent. $B/A = 2\,V_o/V_i$

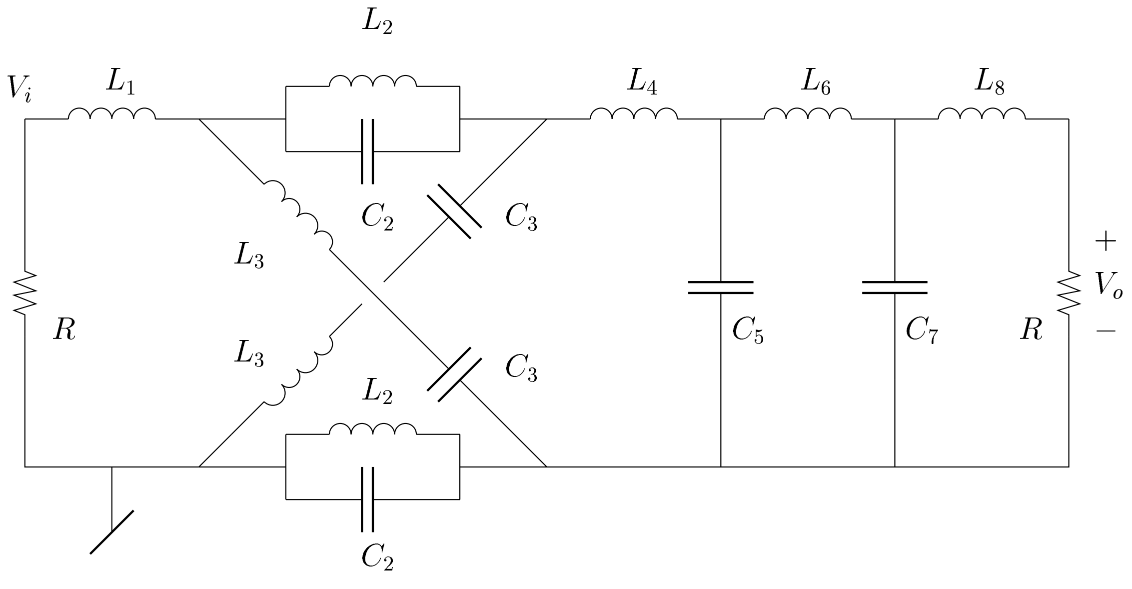

Figure A.2: Linear Phase lowpass filter prototype

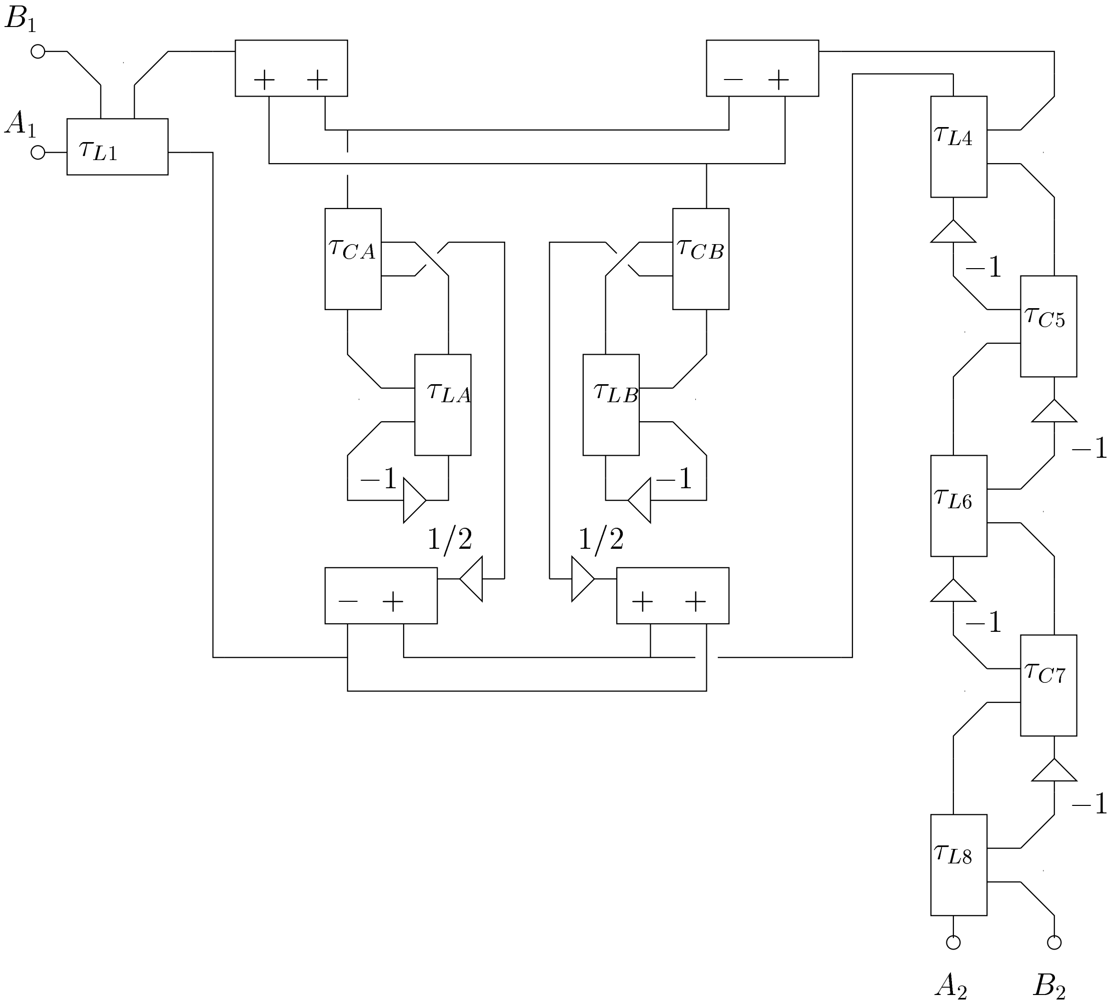

Figure A.3: Wave Active simulation of Linear Phase lowpass filter

Prototype Component	Value	Time constant	C
R	1		
L_1	0.213	$\tau_{L1} = L_1/2 = 0.1065$	22 pF
L_2	2.074	$\tau_{CA} = 2L_2 = 4.1473$	851 pF
C_2	1.013	$\tau_{LA} = C_2/2 = 0.5066$	104 pF
L_3	0.764	$\tau_{LB} = L_3/2 = 0.3822$	78 pF
C_3	2.205	$\tau_{CB} = 2C_3 = 4.4095$	905 pF
L_4	1.142	$\tau_{L4} = L_4/2 = 0.5709$	117 pF
C_5	1.007	$\tau_{C5} = C_5/2 = 0.5036$	103 pF
L_6	2.713	$\tau_{L6} = L_6/2 = 1.3565$	279 pF
C_7	1.156	$\tau_{C7} = C_7/2 = 0.5781$	119 pF
L_8	1.313	$\tau_{L8} = L_8/2 = 0.6566$	135 pF

Table A.1: Component values, time constant expressions and capacitance values for two–pairs in linear phase filter, $G_m = 129$ μA, $F_0 = 100$ kHz

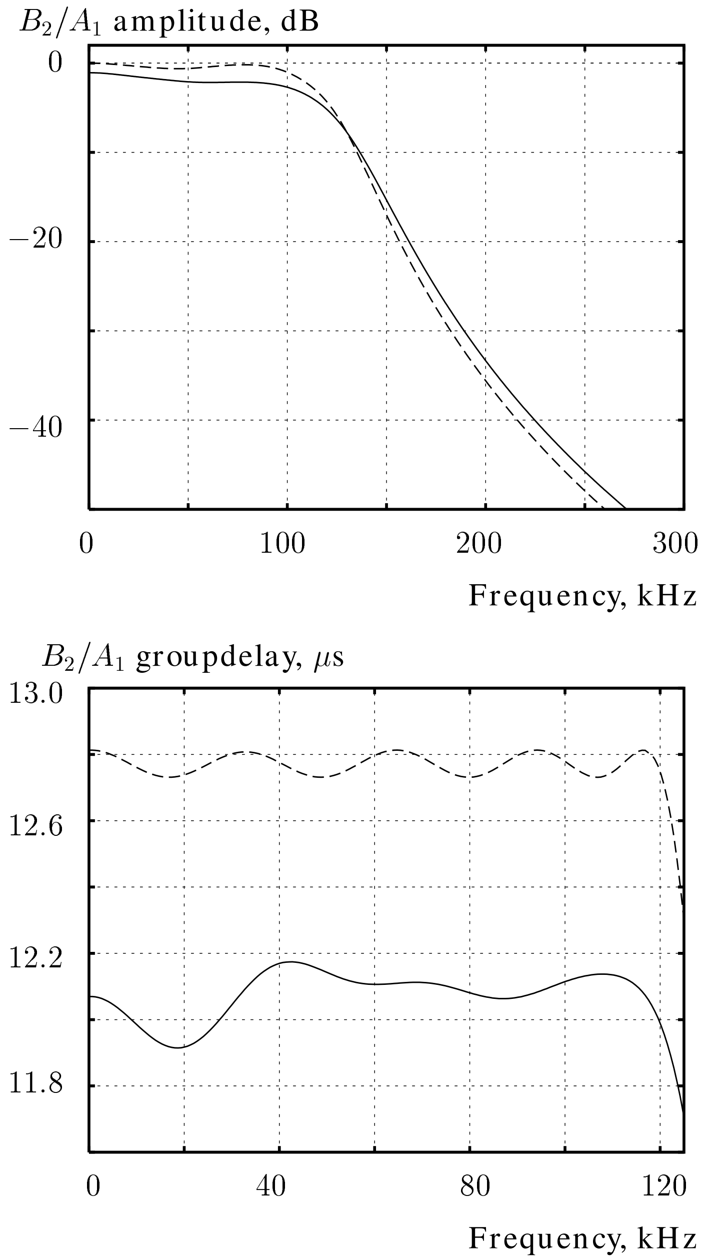

Figure A.4: Transfer function of linear phase lowpass filter, $F_0 = 100$ kHz. Passband group delay and complete amplitude. Solid trace transistorlevel simulation, dotted trace ideal circuit

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Appendix B

The use of symbolic math programs

Many of the mathematical results in chapter 4 were reached by some fairly non–trivial computations. While it would be tempting to treat the effort as just "all part of a day's work", the actual work was mainly done by automatic means, using the computer program `Mathematica` [B.1]. This software package provides symbolic computations and variable precision numerical computations. While there are no really sophisticated mathematical concepts involved in the work presented here, all of the tedious work has been made simpler by the fact that `Mathematica` can do it correctly and quite rapidly. The area where `Mathematica` proves most useful for this thesis is in symbolic matrix computations. The many 2×2 matrices in chapter 4 and appendix C are processed without any problems.

B.1 Brief introduction to `Mathematica` input

The version of `Mathematica`[1] used is a command line driven version for workstations, the input is plain text typed at at command line (or written in a text file which is input automatically). Arrays are input as nested lists, delimited by curly braces. Functions to do linear algebra include `LinearSolve[]` and `Inverse[]`, the function `Simplify[]` attempts to reduce the complexity of an expression and `Together[]` collects all expressions as single fractions.

As an example, I give the input and some output for some Linear Transformation computations. The matrices `cm` and `vm` are transformation matrices for current wave and voltage waves respectively (either $\mathbf{P}$ or $\mathbf{Q}$); `tl` and `tc` are modified chain matrices for a series inductor and a series capacitor respectively. The function `toS[]` accepts a single argument which is supposed to be a 2×2 modified chain matrix ($\mathbf{T}$) matrix and converts into a scattering matrix $\mathbf{S}$, according to equation 3.7. The input data is (with comments delimited by "`(* *)`")

```
(* Current wave matrix *)
cm = {{1/r, 1}, {1/r, -1}};

(* voltage ditto *)
vm = {{1, r}, {1, -r}};
(* Series L arm, T matrix *)
slt = {{1, -s l}, {0, -1}};

(* Par C arm, T matrix *)
pct = {{1, 0}, {s c, -1}};

toS[t_] := Simplify[1/t[[1,2]] {
        {t[[2,2]], -(t[[2,2]] t[[1,1]] - t[[1,2]]t[[2,1]])},
        {1, -t[[1,1]]}}];
```

[1] The version used is V 1.2 for SUN Workstations, later versions is quarantied to produce *identical* output, i.e. the exact expressions shown later will need modification for other versions

Computing the **C** and **S** matrix for the series–L two–pair, the results are (printed out like matrices using `MatrixForm[]`, "`[]`" delimits function arguments, "`[[]]`" indexes arrays, "`%`" indicates previous output):

```
In[4]:= MatrixForm[Together[vm . slt . Inverse[vm]]]

                          -(l s)     2 r + l s
                          ------     ---------
                           2 r         2 r

                          2 r - l s  l s
                          ---------  ---
Out[4]//MatrixForm=         2 r      2 r

In[5]:= MatrixForm[toS[%]]

                             l s        2 r
                          ---------  ---------
                          2 r + l s  2 r + l s

                             2 r        l s
                          ---------  ---------
Out[5]//MatrixForm= 2 r + l s  2 r + l s
```

Here, `Out[4]` is the **C** matrix and `Out[5]` the **S** matrix.

B.2 Finding derivatives of Q and ω

As an example of the use of `Mathematica` to do non–trivial computations, I will show the procedure used to compute the derivatives in section 4.3.2. The main equation used is the derivative of a polynomial zero with respect to a variable which influences the coefficients, in this case τ_d. Setting the nominal polynomial zero to be $P(s, \tau_d) = P(z, 0) = 0$, the derivative of z with respect to

τ_d is simply

$$\frac{\delta z}{\delta \tau_d} = -\left.\frac{\frac{\delta P}{\delta s}}{\frac{\delta P}{\delta \tau_d}}\right|_{(s,\tau_d)=(z,0)} \tag{B.1}$$

(this follows from a simple geometrical argument and assumes that z is a simple zero in P.)

The input starts by setting up the transfer function denominator `lpxds` (Low Pass Transfer Denominator Simplified), by computing the transfer function from the Π matrix which again is the product of the Π matrices for the two components[2].

```
(* Convert to/from Pi matrix from/to S matrix *)
pi2s[pima_] := {
        {pima[[2]][[1]]/pima[[1]][[1]],
        (pima[[1]][[1]]pima[[2]][[2]]
          - pima[[1]][[2]]pima[[2]][[1]])
          / pima[[1]][[1]]},
        {1/pima[[1]][[1]], -pima[[1]][[2]]/pima[[1]][[1]]}}
s2pi[sma_] := {
        {1/sma[[2]][[1]],
         -sma[[2]][[2]]/sma[[2]][[1]]},
        {sma[[1]][[1]]/sma[[2]][[1]],
         (sma[[1]][[2]]sma[[2]][[1]]
           - sma[[1]][[1]]sma[[2]][[2]])
          / sma[[2]][[1]]}}

(* Terms in transfer function matrices *)
alpha = k1 / (1 + s td);
beta = k2 / ((1 + s/a) (1 + s td)^2);

ideal = {k1 -> 1, k2 -> 1, td -> 0}
```

[2] Or something like that. Some confusion about the columns and rows of the Π matrices is evident here. The final results are right. Never mind...

```
(* Pi matrices for two-pairs simulating shunt C and series L *)
badtp1a = Together[s2pi[{{-(alpha - beta), beta},
                         {beta, -(alpha - beta)}}]];

badtp1b = Together[s2pi[{{(alpha - beta), beta},
                         {beta, (alpha - beta)}}]];

lpPi = (badtp1a /. a -> (1/tc)) . (badtp1b /. a -> (1/tl));

(* Convert complete Pi matrix back to S form *)
lpS = pi2s[lpPi];

lpx = Together[lpS[[2,1]]];

(* Only denominator *)
lpxd = 1/lpx[[2]];

(* Insignificant simplification *)
lpxds = lpxd /. {td^3 -> 0, td^4 ->0};

(* Solution for tau == 0 *)
s1t = s /.  Solve[(lpxds /. td -> 0) == 0, s][[1]];

(* Ideal solution *)
s1i = Simplify[s1t /. {k1 -> 1, k2 -> 1}];
```

The result is the zero point `s1i` which is the ideal pole value.

```
                         2                2
      -tc - tl + Sqrt[tc  - 6 tc tl + tl ]
s1i = ------------------------------------
                    4 tc tl
```

The next step is to take the two derivatives using the `D[]` function which produces the derivative of the first argument with respect to the second. The “`/.`” statement performs a substitution, i.e. inserts the condition from equation B.1.

```
ddds = Simplify[D[lpxd, s] /.
        { s -> s1i, k1 -> 1, k2 -> 1, td -> 0}];
dddt = Simplify[D[lpxd, td] /.
        { s -> s1i, k1 -> 1, k2 -> 1, td -> 0}];
dpdt = Simplify[-dddt/ddds];
```

The result of this is a slightly large expression, as follows

```
                 3         2               2        3
dpdt = -(8 tc  - 16 tc  tl - 16 tc tl  + 8 tl  -

                 2        2                2
>       11 tc  Sqrt[tc  - 6 tc tl + tl ] +

                            2                2
>       10 tc tl Sqrt[tc  - 6 tc tl + tl ] -

                 2        2                2         2                2 3/2
>       11 tl  Sqrt[tc  - 6 tc tl + tl ] + 3 (tc  - 6 tc tl + tl )    ) /

               2   2         2                2
>    (32 tc  tl  Sqrt[tc  - 6 tc tl + tl ])
```

The next step is to pick out the real and imaginary parts `pdr` and `pdi` and the real and imaginary parts of the ideal value, `pr` and `pi`. This involves looking at the terms, deciding which are real and which are imaginary — `Mathematica` is not quite able to do this in the version used here — in this case, terms `1`, `2`, `3` and `4` of the numerator are real and become imaginary because of the denominator.

```
pdr = Simplify[(dpdt[[1]] dpdt[[2]] dpdt[[3]] dpdt[[4]]
        (dpdt[[5,5]] + dpdt[[5,6]] + dpdt[[5,7]]
         + dpdt[[5,8]]))];


pdi =  -I (dpdt[[1]] dpdt[[2]] dpdt[[3]] dpdt[[4]]
        (dpdt[[5,1]] + dpdt[[5,2]] + dpdt[[5,3]]
         + dpdt[[5,4]]));


pi = -I (s1i[[1]] s1i[[2]] s1i[[3]] s1i[[4,3]]);
pr = s1i[[1]] s1i[[2]] s1i[[3]]( s1i[[4,1]] +  s1i[[4,2]]);
```

The last step is to take the derivative of the Q and ω functions by inserting the `pr + tau*pdr` expression for the real part (and so on) and taking the derivative using `D[]`.

```
(* Compute Omega-Q from real and imaginary parts *)
omf[r_, i_] := Sqrt[r^2 + i^2];
qf[r_, i_] := -omf[r, i]/(2 r);

dom = Simplify[D[omf[pr + tau*pdr, pi + tau*pdi], tau] /.
       tau -> 0];
dq = Simplify[D[qf[pr + tau*pdr, pi + tau*pdi], tau] /.
       tau -> 0];
```

The results are then as shown in equations (4.13) and (4.14), i.e.

```
In[39]:= dom

        -(Sqrt[2] tc) - Sqrt[2] tl
Out[39]= --------------------------
                   3/2   3/2
               4 tc    tl

In[40]:= dq

Out[40]=

                                     2     2
                                   tc  + tl
>    ----------------------------------------------------------------------
             5/2                        3/2   3/2                      5/2
     Sqrt[2] tc    Sqrt[tl] + 2 Sqrt[2] tc    tl    + Sqrt[2] Sqrt[tc] tl
```

B.3 Conclusion

Through the use of symbolic math software, a considerable amount of grunt work can be eliminated completely. While the tasks for which `Mathematica` has been applied do not exactly stress the abilities, correctness becomes less of a worry. Although all software should be treated with caution, the procedures used for matrix inversion and expression simplification are quite simple. (Note also that the results, e.g. the derivatives above, are often checked with other methods; a simulation using `HSPICE` and a numerical optimisation program were built to confirm the validity of the approximation.)

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Appendix C

Linear Transformation analysis/synthesis

The Linear Transformation (LT) filter analysis/synthesis approach [C.2, C.1] is a general framework for simulating LC ladder type filters. Both leapfrog and Wave Active simulation topologies are special cases of LT simulation approaches. The basic idea is to analyse the prototype filter as a chain of two–ports and use linear combinations of the port quantities as state variables in the simulation. It is obvious how Wave Active filter analysis is a special case of LT analysis, what is less obvious is the fact that by careful choice of variables, it is possible to arrive at certain types of impedance simulation filters. This appendix provides a brief introduction to the LT filter synthesis approach and gives a few results relevant to Wave Active filters using waves other than pure voltage waves.

Taking our definition of port variables — $\mathbf{R^i}$, $\mathbf{V^i}$ and $\mathbf{I^i}$ — from section 3.1, the two sets of variables $[x_1^i \; y_1^i]^T$ and $[x_2^i \; y_2^i]^T$ are defined for section i as follows

$$\begin{bmatrix} x_1^i \\ y_1^i \end{bmatrix} = \mathbf{P^i} \begin{bmatrix} V_1^i \\ I_1^i \end{bmatrix}$$

$$\begin{bmatrix} x_2^i \\ y_2^i \end{bmatrix} = \mathbf{Q^i} \begin{bmatrix} V_2^i \\ I_2^i \end{bmatrix} \tag{C.1}$$

The two transformation matrices $\mathbf{P^i}$ and $\mathbf{Q^i}$ are nonsingular matrices which define the type of linear transformation in use. The matrices $\mathbf{P^i}$ are denoted *left* transformation matrices and $\mathbf{Q^i}$ *right* transformation matrices, for obvious reasons. The $\mathbf{S}$ matrices from which active networks are derived are computed from the $\mathbf{C}$ matrices which again are derived from the transformation matrices and the modified chain matrices $\mathbf{T}$ as follows

$$\begin{aligned}
\begin{bmatrix} V_1^i \\ I_1^i \end{bmatrix} &= \mathbf{T^i} \begin{bmatrix} V_2^i \\ I_2^i \end{bmatrix} \\
\begin{bmatrix} x_1^i \\ y_1^i \end{bmatrix} &= \mathbf{C^i} \begin{bmatrix} x_2^i \\ y_2^i \end{bmatrix} \\
\mathbf{C^i} &= \mathbf{P^i}\,\mathbf{T^i}\,(\mathbf{Q^i})^{-1}
\end{aligned} \tag{C.2}$$

($\mathbf{C}$ matrices are similar to Π matrices from chapter 3, the difference is in the ordering of the elements.) In order that interconnection of adjacent section makes sense, the transformed variables must be compatible, i.e.

$$\begin{bmatrix} x_2^i \\ y_2^i \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} x_1^{i+1} \\ y_1^{i+1} \end{bmatrix} \tag{C.3}$$

(In case of incompatability, an interconnection network must be defined; the matching network is an example of an interconnection network.)

For leapfrog synthesis the following transformation matrices lead to conventional circuits, with section i a series arm and section j a shunt arm

$$\mathbf{P^i} = \begin{bmatrix} \alpha_1^i & 0 \\ 0 & \delta_1^i \end{bmatrix} \quad \mathbf{Q^i} = \begin{bmatrix} \alpha_2^i & 0 \\ 0 & \delta_2^i \end{bmatrix} \tag{C.4}$$

$$\mathbf{P^j} = \begin{bmatrix} 0 & \beta_1^j \\ \gamma_1^j & 0 \end{bmatrix} \quad \mathbf{Q^j} = \begin{bmatrix} 0 & \beta_2^j \\ \gamma_2^j & 0 \end{bmatrix} \tag{C.5}$$

in order for the realisation to be compatible (i.e. for (C.3) to be met), the constants must obey the constraints $\alpha_2^i = \gamma_1^{i+1}$ and $\delta_2^i = -\beta_1^{i+1}$ for a series section i followed by a shunt section $i+1$ (or $\alpha_1^{i+1} = \gamma_2^i$ and $\delta_1^{i+1} = -\beta_2^i$ for shunt followed by series). For $\alpha = \pm 1$, $\gamma = \pm 1$, $\beta = \pm R$ and $\delta = \pm R$ (arranged appropriately) conventional Active–RC leapfrog filters can be synthesised.

Another pair of transformation matrices generates the S matrices known from Wave Active synthesis

$$\mathbf{P^i} = \mathbf{Q^i} = \begin{bmatrix} \alpha & \beta \\ \alpha & -\beta \end{bmatrix} \tag{C.6}$$

with $\alpha = 1$ and $\beta = R$.

C.1 Mixed Wave analysis

In this section, the first letter (if uppercase) of the upper index indicates voltage or current, i.e. $\mathbf{P^{Vi}}$ *is left transformation matrix for voltage waves for section* i*,* $\mathbf{A^{Ij+1}}$ *is current waves for section* $j+1$*,* $\mathbf{S^i}$ *is still the* $\mathbf{S}$ *matrix of section* i*.*

Since both voltage and current state variables are involved in the synthesis of the conventional Voltage Wave S matrix (3.4), it is interesting to consider what happens if we involve both voltage and current *waves* in the analysis. Using curent waves is simply a question of multiplying the definition of voltage waves by $1/R$, i.e. (assuming identical impedance level R throughout)

$$\begin{aligned} \mathbf{A^{Ii}} &= \frac{1}{R}\mathbf{V^i} + \mathbf{I^i} \\ \mathbf{B^{Ii}} &= \frac{1}{R}\mathbf{V^i} - \mathbf{I^i} \end{aligned} \tag{C.7}$$

i.e. $\mathbf{A^{Ii}} = \mathbf{1/R}\,\mathbf{A^{Vi}}$ etc. The transformation matrices for current waves are thus

$$\mathbf{P^{Ii}} = \mathbf{Q^{Ii}} = \begin{bmatrix} 1/R & 1 \\ 1/R & -1 \end{bmatrix} \tag{C.8}$$

Again, the relations to voltage waves are simple, i.e. $\mathbf{P^{Ii}} = \mathbf{1/R\,P^{Vi}}$. The $\mathbf{C}$ matrices for pure current waves are identical to the $\mathbf{C}$ matrices for pure voltage waves since they are related by mutiplication by R/R, i.e.

$$\mathbf{C^{Ii}} = \mathbf{P^{Ii}\,T^{i}\,(Q^{Ii})^{-1}} = \frac{\mathbf{1}}{\mathbf{R}}\mathbf{P^{Vi}\,T^{i}\,R\,(Q^{Vi})^{-1}} = \mathbf{C^{Vi}} \tag{C.9}$$

To investigate the consequences of having different waves at the different terminals of the two–pairs, we look into various options. One possibility is to have the section alternatingly current and voltage waves; this would require transconductance and transimpedance conversion at each intersection (to ensure compatability) but is not otherwise different (indeed, if $R = 1$, the filters are the same as filters derived from analysis with only one type of wave). A slightly more interesting option is to see what happens if the waves at different ends of the two–pair are different, i.e. A_1^i and B_1^i are voltage waves for A_2^i and B_2^i current waves and vice versa. For two consequtive sections, i and $i+1$ with the left waves of section i voltage waves, we get the transformation matrices

$$\begin{aligned} \mathbf{P^{Mi}} &= \begin{bmatrix} 1 & R \\ 1 & -R \end{bmatrix} \quad \mathbf{Q^{Mi}} = \begin{bmatrix} 1/R & 1 \\ 1/R & -1 \end{bmatrix} \\ \mathbf{P^{Mi+1}} &= \begin{bmatrix} 1/R & 1 \\ 1/R & -1 \end{bmatrix} \quad \mathbf{Q^{Mi+1}} = \begin{bmatrix} 1 & R \\ 1 & -R \end{bmatrix} \end{aligned} \tag{C.10}$$

To investigate, we analyse two sections from a polynomial lowpass filter, a series inductor followed by a shunt capacitor. The two modified chain matrices are as follows

$$\begin{aligned} \mathbf{T^i} &= \begin{bmatrix} 1 & -sL \\ 0 & -1 \end{bmatrix} \\ \mathbf{T^{i+1}} &= \begin{bmatrix} 1 & 0 \\ sC & -1 \end{bmatrix} \end{aligned} \tag{C.11}$$

The $\mathbf{S}$ matrix of the circuit simulating section i is then derived from the $\mathbf{C}$ matrix, i.e.

$$\begin{aligned} \mathbf{C^i} &= \mathbf{P^{Mi}}\,\mathbf{T^i}\,(\mathbf{Q^{Mi}})^{-1} = \begin{bmatrix} -sL/2 & R + sL/2 \\ R - sL/2 & sL/2 \end{bmatrix} \\ \mathbf{S^i} &= \frac{\mathbf{1}}{\mathbf{1 + sL/(2R)}} \begin{bmatrix} sL/(2R) & R \\ 1/R & sL/(2R) \end{bmatrix} \end{aligned} \tag{C.12}$$

The next $\mathbf{S}$ matrix is then

$$\begin{aligned} \mathbf{C^{i+1}} &= \begin{bmatrix} sC/2 & 1/R + sC/2 \\ 1/R - sC/2 & -sC/2 \end{bmatrix} \\ \mathbf{S^{i+1}} &= \frac{\mathbf{1}}{\mathbf{1 + sRC/2}} \begin{bmatrix} -sRC/2 & 1/R \\ R & -sRC/2 \end{bmatrix} \end{aligned} \tag{C.13}$$

Another possibility is to make the forward wave voltage and the reflected wave current. This gives us identical transformation matrices for all sections and still no compatability problems.

$$\mathbf{P^{Mi}} = \begin{bmatrix} 1 & R \\ 1/R & -1 \end{bmatrix} \quad \mathbf{Q^{Mi}} = \begin{bmatrix} 1/R & 1 \\ 1 & -R \end{bmatrix} \tag{C.14}$$

The $\mathbf{C}$ and $\mathbf{S}$ matrices for the series inductor are

$$\mathbf{C^i} = \begin{bmatrix} -sL/2 & 1 + sL/(2R) \\ 1 - sL/(2R) & sL/(2R^2) \end{bmatrix}$$

$$\mathbf{S^i} = \frac{\mathbf{1}}{\mathbf{1 + sL/(2R)}} \begin{bmatrix} sL/(2R^2) & 1 \\ 1 & sL/2 \end{bmatrix} \tag{C.15}$$

and for the shunt capacitor they are

$$\mathbf{C^i} = \begin{bmatrix} sR^2C/2 & 1 + sRC/2 \\ 1 - sRC/2 & -sC/2 \end{bmatrix}$$

$$\mathbf{S^{i+1}} = \frac{\mathbf{1}}{\mathbf{1 + sRC/2}} \begin{bmatrix} -sC/2 & 1 \\ 1 & -sR^2C/2 \end{bmatrix} \tag{C.16}$$

For both of the Mixed Wave analysis approaches, the modifications — compared to pure wave analysis — are simply that some elements of the two–pair transfer funcntions get scaled by R. In the simple case where $R = 1$, this makes no difference. The more interesting case, where $R = 1/G_m$, is problematic since the same input is used both impedance scaled and not impedance scaled. In other words, there does not seem to be a simple method by which mixed signal analysis can be used in the implementation (or, more accurately, analysis with Mixed Waves does not inspire me to any new and better circuits).

References

[C.1] A M Ali. Further results on the design of active filters by linear transformation. In *Proceedings of the International Symposium on Circuits and Systems*, pages 553 – 556. IEEE, 1980.

[C.2] H G Dimopoulos and A G Constantinides. Linear transformation active filters. *IEEE Transactions CAS*, 25(10):845 – 852, 1978.

Appendix D

GaAs integrated filter

As part of the literature study, I stumbled over a paper where a Signal Flow Graph (SFG) showed the correct configuration for a Wave Active biquad. As such I feel it should be included in this thesis, even though the actual filter is not a Wave Active filter (as far as I can make out...).

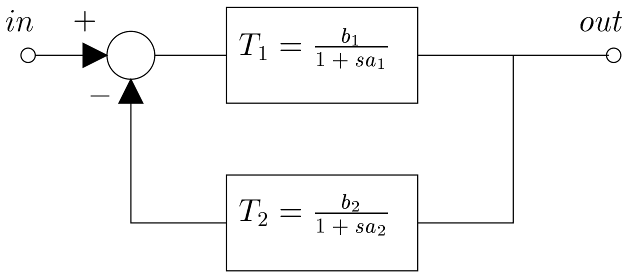

Figure D.1: SFG of "new active" filter biquad

The GaAs technology filter in [D.1] is claimed to use bandpass biquads composed of two lossy integrators in a feedback arrangement. This is exactly the configuration of a Wave Active simulation of a bandpass biquad for the A_2 input zero and the B_1 output not realised. To form a fourth order bandpass filter, two biquads are cascaded. The SFG shown in the paper is given in figure D.1.

On the other hand, the filter implementation shown in the paper does *not*

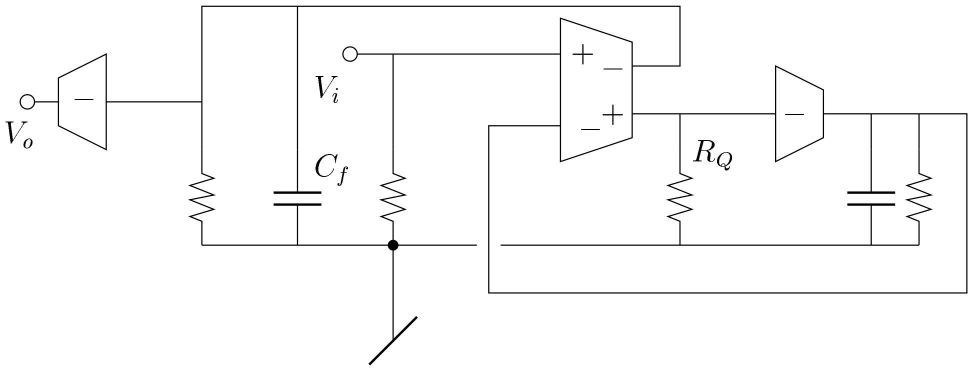

Figure D.2: Topology of GaAs "new active" biquad

have a feedback connection from the output. The OTA–RC equivalent is (attempted) reproduced in figure D.2 and comes across as a gyrator–C filter with resistive loading of both capacitors. The current amplifier (R_Q plus OTA) makes the gyrator active. By altering the value of C_f, one reactive component is tuned; using R_Q, the other reactive component (simulated inductor) is tuned. As the resistive loading is constant, a tuning of both reactive elements allow for both centre frequency and Q tuning. The filter operates in a $50\,\Omega$ environment (hence the "current" output). For the fourth order filter described in the paper the two biquads must be tuned separately. The tuning ranges are quite adequate, with Q tuning range greater than $20 - 200$ and the centre frequency more than 0.1 GHz around 1.3 GHz. The flat level of the transfer function changes with frequency tuning and both the centre frequency and the Q factor depend on both tuning quantities. This filter exhibits one characteristic of other Wave Active filters: the ability to have high Q factor without having high gain OTAs. Unfortunately, the tuning process is quite intricate; e.g. there does not appear to be a simple process by which high order filters (cascades of biquads with different $\omega - Q$ values) can be tuned from only one pair of tuning voltages.

While the results are quite impressive, the actual circuit does *not* implement the SFG given; the filter is therefore not a Wave Active filter.

References

[D.1] H Suwaki and T Ohira. A very small MMIC variable filter based on a new active filter design concept. In *Proceedings of the GaAs IC symposium*, pages 93 – 96, 1990.

Appendix E

Measurement equipment and procedure

This appendix describes the measurements of the CMOS intergrated chip described in section 5.2.